PENGUIN™
SOLUTIONS

Penguin Edge™ ATCA-7480 Series

Installation and Use Manual

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EDGE

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About this Manual

Overview of Contents

This guide is intended for the users qualified in electronics or electrical engineering. Users must have a working understanding of Peripheral Component Interconnect (PCI), AdvancedTCA®, and telecommunications.

The manual contains the following chapters and appendices:

About this Manual on page 21 lists the conventions and abbreviations used in this manual and outlines the revision history.

Safety Notes on page 27 lists safety notes applicable to the blade.

Notice de Sécurité on page 35 provides the French translation of the safety notes section.

Sicherheitshinweise on page 41 provides the German translation of the safety notes section.

Chapter 1, Introduction on page 49 describes the main features, mechanical data, and ordering information of the blade.

Chapter 2, Hardware Preparation and Installation on page 53 outlines the installation requirements, hardware accessories, switch settings, installation and removal procedures.

Chapter 3, Controls, Indicators, and Connectors on page 73 describes external interfaces of the blade. This includes connectors and LEDs.

Chapter 4, Functional Description on page 89 describes the functional blocks of the blade in detail. This includes a block diagram, description of the main components used and so on.

Chapter 5, Maps and Registers on page 107 provides information about the maps and registers of the blade.

Chapter 6, BIOS on page 175 describes the features and setup of BIOS.

Chapter 7, Serial Over LAN on page 225 provides information on how to establish a serial-over LAN session on your blade.

Chapter 8, Supported IPMI Commands on page 231 lists all supported IPMI commands.

Chapter 9, IPMI Feature Set on page 281 provides information about controlling via IPMI.

Appendix A, Ruggedized ATCA-7480 Information on page 323 provides ATCA-7480-D information.

Appendix B, Related Documentation on page 327 provides links to related documentation.

Abbreviations

This document uses the following abbreviations:

Abbreviation	Definition
APIC	Advanced Programmable Interrupt Controller
ATA	Advanced Technology Attachment
ATCA	Advanced Telecommunications Computing Architecture
BIOS	Basic Input/Output System
DDR	Double Data Rate
DIMM	Dual Inline Memory Module
DMA	Direct Memory Access
DMI	Direct Media Interface
ECC	Error-Correction Code
EMC	Electromagnetic Compatibility
EMV	Elektromagnetische Vertraeglichkeit
EN	European Norm
ESD	Electrostatic Sensitive Device
FPGA	Field-Programmable Gate Array
IIO	Intel Integrated I/O
IOAPIC	Intel I/O Advanced Programmable Interrupt Controller
IPMB	Intelligent Platform Management Bus
IPMC	Intelligent Platform Management Controller
IPMI	Intelligent Platform Management Interface
ISA	Industry Standard Architecture
MAC	Media Access Control
NEBS	Network Equipment Building System
NVRAM	Nonvolatile Random Access Memory
OEM	Original Equipment Manufacturer
OOS	Out-Of-Service

Abbreviation	Definition
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PCIe	PCI Express
PCU	Processor Power Control Unit
PEM	Power Entry Module
PICMG	PCI Industrial Computer Manufacturers Group
PIM	Power Input Module
PMC	PCI Mezzanine Card
POST	Power-On Self-Test
PROM	Programmable Read-Only Memory
QPI	Intel QuickPath Interconnect
RAS	Reliability and Serviceability
RTC	Real Time Clock
RTM	Rear Transition Module
RoHS	Restriction of the use of Certain Hazardous Substances
SAS	Serial Attached SCSI
SATA	Serial ATA
SCSI	Small Computer System Interface
SDR	Sensor Data Record
SMI	Serial Management Interface
SOL	Serial-over-LAN
SPD	Serial Presence Detect
SPI	Serial Peripheral Interface
SSC	Spread Spectrum Clocking
VLP	Very Low Profile
VGA	Video Graphics Adapter

Conventions

The following table describes the conventions used throughout this manual.

Notation	Description
`0x00000000`	Typical notation for hexadecimal numbers (digits are 0 through F), for example used for addresses and offsets
`0b0000`	Same for binary numbers (digits are 0 and 1)
bold	Used to emphasize a word
`Screen`	Used for on-screen output and code related elements or commands in body text
`Courier + Bold`	Used to characterize user input and to separate it from system output
Reference	Used for references and for table and figure descriptions
File > Exit	Notation for selecting a submenu
<text>	Notation for variables and keys
[text]	Notation for software buttons to click on the screen and parameter description
...	Repeated item for example node 1, node 2, ..., node 12
. . .	Omission of information from example/command that is not necessary at the time being
..	Ranges, for example: 0..4 means one of the integers 0,1,2,3, and 4 (used in registers)
|	Logical OR
	Indicates a hazardous situation which could result in death or serious injury
	Indicates a hazardous situation whichmay result in minor or moderate injury

Notation	Description
	Indicates a property or equipment damage message
	Indicates an electrical situation that could result in moderate injury or death
	Indicates that when working in an ESD environment care should be taken to use proper ESD practices
	Pay attention to important information. No Danger encountered.

Summary of Changes

This manual has been revised and replaces all prior editions. S

Part Number	Publication Date	Description
6806800T17M	July 2022	Rebranded to Penguin Solutions.Updated Section 1.1 Overview. Updated Appendix A title and Section A.1; updated Table B-1 for related documentation. Updated Support web page url throughout document.
6806800T17L	May 2021	Updated Section 2.4 Switch Settings; added Table 2-8 Switch SW100 Settings; updated Section 5.1.11.2 and 9.4.9 to update Manual Powering info for the SW100.1 switch.
6806800T17K	January 2021	Updated Safety Notes and Table 1-1 for 62368-1 compliance.

Part Number	Publication Date	Description
6806800T17J	September 2019	Rebranded to SMART Embedded Computing. Updated title to "Series". Added Chapter 1, Section 1.2 Standard Compliances. Updated Chapter 4, Sections 4.5 and 4.6 headings were updated. Added MAC Address Assignment table. Updated Conventions Table. Added Appendix for ATCA-7480-D information, renumbered existing appendices. Added data sheets to Related Documentation table. Updated English and German safety notes; added French safety notes section.
6806800T17H	December 2018	Updated *Block Diagram* on page 83.
6806800T17G	September 2016	Updated Table 2-5 on page 49, Figure 4-2 on page 90 and Chapter 6, *BIOS,* on page 181.
6806800T17F	June 2016	Added Figure 3-11 on page 77 and Figure 3-12 on page 77 showing P22 Backplane connector pinout.
6806800T17E	May 2016	Removed Declaration of Conformity.
6806800T17D	September 2015	Added a notice under sections *Installation* on page 28 and *Installation* on page 32. Updated Figure "ATCA-7480 Blade Layout" on page 48, *and* Figure "ATCA-7480 Block Diagram" on page 83.
6806800T17C	June 2015	Added a section *ATCA Update Channels* on page 88. Added Figure "Fail Protect" on page 341. Updated Table 2-7 on page 50, Table 6-7 on page 204, Table 6-13 on page 212, Table 6-20 on page 225, Table 6-21 on page 226, Table 8-14 on page 255, Table 8-15 on page 264 and Table 9-2 on page 312. Updated the section *Runtime Error Logging* on page 225.
6806800T17B	April 2015	Updated Sensor number 32 in Table "ATCA-7480 Specific Sensors" on page 312. Added Table "SOL Channels" on page 239.
6806800T17A	February 2015	Initial Version

Safety Notes

This section provides warnings that precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed during all phases of operation, service, and repair of this equipment. You should also employ all other safety precautions necessary for the operation of the equipment in your operating environment. Failure to comply with these precautions or with specific warnings elsewhere in this manual could result in personal injury or damage to the equipment.

Penguin Solutions intends to provide all necessary information to install and handle the product in this manual. Because of the complexity of this product and its various uses, we do not guarantee that the given information is complete. If you need additional information, ask your Penguin Solutions representative.

The product has been designed to meet the standard industrial safety requirements. It must not be used in safety critical components, life supporting devices or on aircraft.

Only personnel trained by Penguin Solutionsor persons qualified in electronics or electrical engineering are authorized to install, remove or maintain the product. The information given in this manual is meant to complete the knowledge of a specialist and must not be used as replacement for qualified personnel.

Keep away from live circuits inside the equipment. Operating personnel must not remove equipment covers. Only factory authorized service personnel or other qualified service personnel is allowed to remove equipment covers for internal subassembly or component replacement or any internal adjustment.

Do not install substitute parts or perform any unauthorized modification of the equipment or the warranty may be voided. Contact your local Penguin Solutions representative for service and repair to make sure that all safety features are maintained.

EMC

The product has been tested in a standard Penguin Edge™ system and found to comply with the limits for a Class A digital device in this system, pursuant to part 15 of the FCC Rules, EN 55022 Class A respectively. These limits are designed to provide reasonable protection against harmful interference when the product is operated in a commercial, business or industrial environment. The product conducts, radiates and uses radio frequency energy and, if not installed properly and used in accordance with this user documentation, may cause harmful interference to radio communications.

Operating the product in a residential area is likely to cause harmful interference. If this occurs, the user will be required to correct the interference at the user's expense. Changes or modifications not expressly approved by Penguin Solutions could void the user's authority to operate the equipment. Board products are tested in a representative system to show compliance with the above mentioned requirements. A proper installation in a compliant system will maintain the required performance.

Use only shielded cables when connecting peripherals to help assure that appropriate radio frequency emissions compliance is maintained. For proper EMC shielding, only operate the system with face plates installed and all vacant slots covered or populated with filler cards.

The COM, ETH1, ETH2, USB1 and USB2 interfaces are considered debug/maintenance ports. During normal operation, no cables should be connected to these ports. Cables attached to these ports during maintenance must not exceed a length of 10 feet (3 meters).

VCCI

This is a Class A product based on the standard of the Voluntary Control Council for Interference (VCCI) by Information Technology Interference. If this equipment is used in a domestic environment, radio disturbance may arise. When such trouble occurs, the user may be required to take corrective actions.

Grounding

If the product is not properly grounded, it may be damaged by electrostatic discharge.

The system contains EMI gaskets at the shelf and module level. Make sure that each of the system's parts contact the EMI gasket.

The shelf is also fitted with an ESD jack/snap for use with conductive wrist straps. Make sure the operator uses proper ESD protection.

Installation

Personal Injury

This product operates with dangerous voltages that can cause injury or death. Use extreme caution when handling, testing, and adjusting this equipment and its components.

Damage of Circuits

Electrostatic discharge and incorrect product installation and removal can damage circuits or shorten their life.

Before touching the product make sure that you are working in an ESD-safe environment or wearing an ESD wrist strap or ESD shoes. Hold the product by its edges and do not touch any components or circuits.

Data Loss

Wait until the blue LED is permanently illuminated before removing the blade. Removing the blade with the blue LED still blinking causes data loss.

Restricted Access Area

This product is only to be installed in a restricted access area.

Damage of the Blade and Additional Devices and Modules

Before installing or removing an additional device or module, read the respective documentation.

Incorrect installation of additional devices or modules may damage the product or the additional devices or modules.

Blade Damage

Incorrect installation of the blade can cause damage to the blade.

Use handles when installing/removing the blade to avoid damage/deformation to the face plate and/or PCB.

Damage to Blade/Backplane or System Components

Bent pins or loose components can cause damage to the blade, the backplane, or other system components. Carefully inspect the blade and the backplane for both pin and component integrity before installation.

Penguin Solutions and our suppliers take significant steps to make sure that there are no bent pins on the backplane or connector damage to the blades prior to leaving the factory. Bent pins caused by improper installation or by inserting boards with damaged connectors could void the warranty for the backplane or blades.

System Damage

WARNING: The intra-building port (s) of the equipment or subassembly is suitable for connection to intra-building or unexposed wiring or cabling only. The intra-building port (s) of the equipment or subassembly MUST NOT be metallically connected to interfaces that connect to the outside plant (OSP) or its wiring. These interfaces are designed for use as intra-building interfaces only (Type 2 or Type 4 ports as described in GR-1089) and require isolation from the exposed OSP cabling. The addition of primary protectors is not sufficient protection in order to connect these interfaces metallically to OSP wiring.

The intra-building port (s) of the equipment or subassembly must use shielded intra-building cabling/wiring that is grounded at both ends.

Rear Transition Module

Damage of the RTM

Incorrect installation of the RTM can cause damage to the RTM.

Use handles when installing/removing the RTM to avoid damage/deformation to the face plate and/or PCB.

Damage to RTM/Backplane or System Components

Bent pins or loose components can cause damage to the RTM, the backplane, or other system components. Carefully inspect the RTM and the backplane for both pin and component integrity before installation.

Penguin Solutions and our suppliers take significant steps to ensure there are no bent pins on the backplane or connector damage to the blades/RTMs prior to leaving the factory. Bent pins caused by improper installation or by inserting blades with damaged connectors could void the warranty for the backplane or blades.

Operation

Make sure that the display devices that are permanently connected to the VGA interface provide a fire enclosure according to the IEC/EN/UL/CSA 62368 and 60950-1 requirements.

All other devices that are only connected to the VGA interface for service purposes need supervision during operation and must be disconnected after maintenance.

Product Damage - Product Surface

High humidity and condensation on the product surface causes short circuits.

Do not operate the product outside the specified environmental limits. Make sure the product is completely dry and there is no moisture on any surface before applying power.

Overheating and Blade Damage

When operating the product, make sure that forced air cooling is available in the shelf or enclosure. Operating the product without forced air cooling may lead to overheating and product damage. When operating the product in areas of electromagnetic radiation, secure the product in the system using the front panel screws. Make sure the product is fully shielded by the enclosure.

Data Corruption

If power to the unit is removed while a firmware update is in progress to the product's flash memory, the changes will not be saved or the flash memory may be corrupted. In such case, the product is likely to remain in a non-operable state and will require reconditioning by qualified repair services.

Injuries or Short Circuits - Blade or Power Supply

In case the OR-ing diodes of the blade fail, the blade may trigger a short circuit between input line A and input line B so that input line A remains powered even if it is disconnected from the power supply circuit (and vice versa).To avoid damage or injuries, always check that there is no voltage on the line that has been disconnected before continuing your work.

The EMI radiation compliancy of the product has been qualified in a reference system with 10 ATCA-7480 boards installed each with the Spread Spectrum feature enabled. Please note that the integrator needs to verify the EMI radiation compliancy of other configurations/settings (for example, Spread Spectrum disabled).

Switch Settings

Product Malfunction

Do not change settings of switches marked as **Reserved**. Switches marked **Reserved** might carry production-related functions and can cause the product to malfunction if their setting is changed.

Check and change the setting of any switch not marked **Reserved** before installing the product.

Product Damage

Check and change switch settings before you install the product.

Setting/resetting the switches during operation can cause damage to the product.

Use minimal force when pressing the reset switch. Too much force may damage the reset switch.

RJ-45 Connector

System Damage

RJ-45 connectors on the front panel are either twisted-pair Ethernet (TPE) or E1/T1/J1 network interfaces. Connecting an E1/T1/J1 line to an Ethernet connector may damage your system.

- Make sure that TPE connectors near your working area are clearly marked as network connectors.
- Verify that the length of an electric cable connected to a TPE bushing does not exceed 100 meters or approximately 328 feet.
- Make sure the TPE bushing of the system is connected only to safety extra low voltage circuits (SELV circuits).
- If in doubt, ask your system administrator.

For more information, see the documentation of the respective product.

Hot Swap

Data Loss

Wait until the blue LED is permanently illuminated before removing the product. Removing the product with the blue LED still blinking causes data loss.

Laser

Personal Injury

If a label with the words CLASS 1 LASER PRODUCT is affixed to your system, the unit is equipped with a laser device. These devices contain a laser system that produces visible or invisible laser radiation (or both) and can be harmful to the eyes.

Seek supplemental information (power, wavelength, visibility, pulse duration, applicable standards) prior to servicing equipment. Do not look at laser device with an optical instrument at any time.

Battery

Blade Damage

Incorrect battery installation may result in a hazardous explosion and blade damage.

Always use the same type of lithium battery as is installed and make sure the battery is installed as described in the manual.

Data Loss

Installing another battery type than the one mounted at product delivery may cause data loss.

PCB and Battery Holder Damage

Do not use a screw driver to remove the battery from its holder. Removing the battery with a screw driver may damage the PCB or the battery holder.

Environment

Environmental Damage

Improper disposal of used products may harm the environment.

Always dispose of used products according to your country’s legislation and manufacturer’s instructions.

Notice de Sécurité

Cette section présente, à travers ce manuel, des avertissements qui précèdent les procédures potentiellement dangereuses. Les instructions contenues dans les avertissements doivent être suivies durant toutes les phases d'opération, de service et de réparation de cet équipement. Vous devriez aussi employer toute autre précaution nécessaire pour l'utilisation de l'équipement dans l'environnement d'opération. Le défaut de se conformer à ces précautions ou aux avertissements spécifiques contenus ailleurs dans ce manuel, peut engendrer des lésions corporelles ou dommages à l'équipement.

Penguin Solutions™ prévoit dans ce manuel de fournir toute l'information nécessaire pour installer et manipuler le produit. En raison de la complexité de ce produit et de ses diverses utilisations, nous ne pouvons pas garantir que les informations fournies sont complètes. Si vous avez besoin d'information supplémentaire, contactez votre représentant Penguin Solutions.

Le produit a été conçu pour répondre aux exigences de sécurité standards de l'industrie. Il ne doit pas être utilisé dans des composantes critiques pour la sécurité, des appareils de maintien de vie ou sur un aéronef.

Seul le personnel formé par Penguin Solutions ou les personnes qualifiées dans le domaine de l'électronique ou du génie électrique sont autorisés à installer, retirer ou faire l'entretien du produit. Les informations contenues dans ce manuel sont destinées à compléter les connaissances d'un spécialiste et ne peuvent être utilisées en remplacement de personnel qualifié.

Ne touchez pas les circuits sous tension à l'intérieur de l'équipement. Le personnel d'opération ne doit pas enlever les couvercles de l'équipement. Seul le personnel de maintenance autorisé par l'usine ou autre personnel de maintenance qualifié peut retirer les couvercles des équipements pour le sous-assemblage interne ou pour le remplacement de composantes, ou pour tout réglage interne.

N'installez aucune pièce de remplacement et n'effectuez aucune modification non autorisée de l'équipement, sinon, la garantie pourrait être annulée. Contactez votre représentant Penguin Solutions local pour le service et la réparation, afin de vous assurer que toutes les fonctions de sécurité soient maintenues.

Compatibilité électromagnétique (CEM)

Le produit a été testé dans un système Penguin Edge™ standard et est déclaré conforme aux limites imposées à un appareil numérique de classe A dans ce système, conformément à la section 15 de la Réglementation FCC, EN 55022 classe A, respectivement. Ces limites sont conçues pour offrir une protection raisonnable contre les interférences néfastes lorsque le produit est utilisé dans un environnement commercial ou industriel. Le produit conduit, émet et utilise de l'énergie à radiofréquence et, s'il n'est pas installé correctement et utilisé conformément à cette documentation de l'utilisateur, il peut causer des interférences néfastes aux communications radio.

Opérer ce produit dans une région résidentielle est susceptible de causer des interférences néfastes. Si cela se produit, l'utilisateur devra corriger les interférences à ses frais. Les changements ou les modifications qui ne sont pas expressément approuvés par Penguin Solutions pourraient annuler la conformité réglementaire de l'utilisateur. Les cartes sont testées dans un système représentatif pour démontrer la conformité aux exigences mentionnées ci-dessus. Une installation adéquate dans un système conforme maintiendra les performances requises.

Utilisez uniquement des câbles blindés lorsque vous connectez des périphériques pour vous assurer que la conformité aux normes d'émission de radiofréquences est respectée. Pour un blindage CEM adéquat, utilisez le système uniquement avec les plaques frontales installées et tous les ports d'extension vacants couverts ou équipés de cartes obturatrices.

Les interfaces COM, ETH1, ETH2, USB1, USB2 sont considérées comme des ports de débogage/maintenance. Durant une opération normale, aucun câble ne devrait être connecté à ces ports. Les câbles attachés à ces ports pendant la maintenance ne doivent pas excéder une longueur de 10 pieds (3 mètres).

VCCI

Ceci est un produit de classe A basé sur la norme du Conseil volontaire de contrôle des interférences (VCCI) par Information Technology Interference (Interférence des technologies de l'information). Si cet équipement est utilisé dans un environnement domestique, des perturbations radio peuvent survenir. Lorsque de tels problèmes surviennent, l'utilisateur peut être amené à prendre des mesures correctrices.

Mise à la terre

ISi le produit n'est pas adéquatement mis à la terre, il peut être endommagé par une décharge électrostatique.

Le système contient des joints EMI au niveau des étagères et des modules. Assurez-vous que chacune des pièces du système est en contact avec le joint EMI.

L'étagère est également équipée d'une prise/déclic ESD pour une utilisation avec des dragonnes conductrices. Assurez-vous que l'opérateur utilise la protection de décharge électrostatique ESD appropriée.

Installation

Lésions corporelles

Ce produit opère à des voltages dangereux qui peuvent causer des blessures ou la mort. Faites preuve de prudence lorsque vous manipulez, testez ou ajustez l'équipement et ses composantes.

Endommagement des circuits

Les décharges électrostatiques, ainsi que l'installation inadéquate et le retrait du produit peuvent endommager les circuits ou réduire leur durée de vie.

Avant de toucher le produit, assurez-vous que vous travaillez dans un environnement exempt de décharge électrostatique. Tenez le produit par ses extrémités et ne touchez aucune composante ou circuit.

Perte de données

Attendez jusqu'à ce que le DEL bleu soit illuminé de façon permanente avant de retirer la lame.

Retirer la lame lorsque le DEL bleu continue de clignoter peut causer une perte de données.

Zone à accès restreint

Ce produit peut seulement être installé dans les zones à accès restreint.

Endommagement de la lame et appareils ou modules supplémentaires

Avant d'installer ou de retirer un appareil ou un module supplémentaire, lisez la documentation appropriée.

Une installation inadéquate d'appareils ou modules supplémentaires peut endommager la lame ou les appareils ou modules supplémentaires.

Endommagement de la lame

Une installation inadéquate de la lame peut lui causer des dommages.

Utilisez les poignées lorsque vous installez/retirez la lame pour éviter un dommage/déformation de la plaque frontale et/ou PCB.

Dommage à la lame/fond de panier ou aux composantes du système

Des broches tordues ou des composantes desserrées peuvent causer des dommages à la lame, au fond de panier ou à d'autres composantes du système. Inspectez soigneusement la lame et le fond de panier pour vérifier l'intégrité des broches et des composantes avant l'installation.

Penguin Solutions et ses fournisseurs prennent des mesures significatives pour s'assurer qu'il n'y ait pas de broches tordues sur le fond de panier ou qu'il n'y ait pas de dommages de connecteur à la lame avant de quitter l'usine. Des broches tordues causées par une installation inadéquate ou par l'insertion de cartes avec des connecteurs endommagés pourraient annuler la garantie pour le fond de panier ou les lames.

Endommagement du système

AVERTISSEMENT: le port intra-bâtiment de l'équipement ou du sous-ensemble convient uniquement pour la connexion à un câblage intra-bâtiment ou à un filage non exposé uniquement. Le port intra-bâtiment de l'équipement ou du sous-ensemble NE DOIT PAS être relié métalliquement à des interfaces qui se connectent à l'installation extérieure (OSP) ou à son filage. Ces interfaces sont conçues pour être utilisées uniquement comme interfaces intra-bâtiment (ports de type 2 ou de type 4 décrits dans le document GR-1089) et nécessitent une isolation du câblage OSP exposé. L'ajout de protecteurs primaires ne constitue pas une protection suffisante pour connecter ces interfaces de manière métallique au câblage OSP.

Le port intra-bâtiment de l'équipement ou du sous-ensemble doit utiliser un filage/câblage intra-bâtiment blindé mis à la terre aux deux extrémités.

Modules de Transition Arriére (MTA)

Endommagement du MTA

Une installation inadéquate du MTA peut causer des dommages au MTA.

Utilisez les poignées lorsque vous installez/retirez le MTA pour éviter les dommages/déformation de la plaque frontale et/ou du PCB.

Endommagement du MTA/ du fond de panier ou des composants du système

Des broches tordues ou des composants desserrés peuvent causer des dommages au MTA, au fond de panier ou autres composants du système. Inspectez soigneusement le MTA et le fond de panier pour vérifier l’intégrité des broches et des composantes avant l’installation.

Penguin Solutions et ses fournisseurs prennent des mesures significatives pour s'assurer qu’il n’y ait pas de broches tordues sur le fond de panier ou qu’il n’y ait pas de dommages de connecteur à la lame/MTA avant de quitter l’usine. Des broches tordues causées par une installation inadéquate ou par l’insertion de cartes avec des connecteurs endommagés pourraient annuler la garantie pour le fond de panier ou les lames.

Opération

Assurez-vous que les appareils d’affichage qui sont connectés en permanence à l’interface VGA offrent un boîtier anti-incendie conforme aux exigences IEC/EN/UL/CSA 62368-1 et 60950-1.

Tous les autres appareils qui sont seulement connectés à l'interface VGA à des fins de maintenance doivent être surveillés durant l’opération et doivent être déconnectés après la maintenance.

Endommagement du produit – Surface du produit

Une humidité élevée ou la condensation sur la surface du produit cause des courts-circuits.

Ne pas opérer le produit en dehors des limites environnementales spécifiées. Assurez-vous que le produit soit complètement sec et qu'il n'y ait aucune humidité sur aucune surface avant de mettre en marche.

Surchauffe et endommagement du produit

Lorsque vous opérez le produit, assurez-vous qu'un refroidissement par air forcé est disponible dans l'étagère ou le boîtier.

Opérer le produit sans refroidissement par air forcé peut mener à une surchauffe et un endommagement du produit.

Lorsque vous opérez le produit dans des régions de rayonnement électromagnétique, sécurisez le produit dans le système en utilisant les vis du panneau avant. Assurez-vous que le produit soit entièrement protégé par le boîtier.

Corruption des données

Si l'appareil est mis hors tension alors qu'une mise à jour du microprogramme est en cours dans la mémoire flash du produit, les modifications ne seront pas enregistrées ou la mémoire flash pourrait être corrompue. Dans un tel cas, le produit restera probablement dans un état inutilisable et nécessitera un reconditionnement par des services de réparation qualifiés.

Blessures ou courts-circuits – Lame ou source de courant

Si les diodes O-Ring de la lame tombent en panne, la lame peut déclencher un court-circuit entre la ligne d'entrée A et la ligne d'entrée B, de sorte que la ligne A reste alimentée même si elle est déconnectée du circuit d'alimentation (et inversement).

Pour éviter tout dommage ou blessure, vérifiez toujours qu'il n'y ait aucun voltage sur la ligne qui a été déconnectée avant de continuer votre travail.

La conformité du produit aux rayonnements EMI a été qualifiée dans un système de référence avec 10 cartes ATCA-7480 installées chacune avec la fonction Spread Spectrum activée. Veuillez noter que l'intégrateur doit vérifier la conformité aux rayonnements EMI d'autres configurations/réglages (par exemple, Spread Spectrum désactivée).

Modifier les Paramètres

Mauvais fonctionnement du produit

Ne modifiez pas les configurations des commutateurs marqués **Reserved**. Les commutateurs marqués **Reserved** peuvent comporter des fonctions liées à la production et entraîner un mauvais fonctionnement du produit si les paramètres sont modifiés.

Vérifiez et modifiez les paramètres de tout commutateur non marqué **Reserved** avant d'installer le produit.

Endommagement du produit

Vérifiez et modifiez les paramètres du commutateur avant d'installer le produit.

Le configuration/réinitialisation des commutateurs pendant le fonctionnement peut causer des dommages au produit.

Utilisez une force minimale lorsque vous appuyez sur le commutateur de réinitialisation. Une force excessive pourrait endommager le commutateur de réinitialisation.

Les Connecteurs RJ-45

Endommagement du système

Les connecteurs RJ-45 situés sur le panneau avant sont des interfaces réseau Ethernet à paire torsadée (TPE) ou E1/T1/J1. La connexion d'une ligne E1 / T1 / J1 à un connecteur Ethernet peut endommager votre système.

- Assurez-vous que les connecteurs TPE situés près de votre zone de travail soient clairement identifiés comme étant des connecteurs réseau.
- Vérifiez que la longueur d'un câble Ethernet connecté à un connecteur TPE ne dépasse pas 100 mètres (environ 328 pieds).
- Assurez-vous que le connecteur TPE du système soit uniquement connecté aux circuits de sécurité très basse tension (SELV).
- En cas de doute, demandez à votre administrateur de système.

Pour plus d'informations, voir la documentation du produit respectif.

Hot Swap

Perte de données

Attendez jusqu’à ce que le DEL bleu soit illuminé de façon permanente avant de retirer la lame. Retirer la lame lorsque le DEL bleu continue de clignoter peut causer une perte de données.

Laser

Lésions corporelles

Si une étiquette avec les mots PRODUIT LASER DE CLASSE 1 est apposée sur votre système, l'unité est équipée d'un appareil laser. Ces appareils contiennent un système laser qui produit des rayonnements visibles ou invisibles (ou les deux) et peut être nocif pour les yeux.

Recherchez de l'information supplémentaire (puissance, longueur d'onde, visibilité, durée d'impulsion, normes applicables) avant de faire le maintien de l'équipement. Ne regardez jamais un appareil laser avec un instrument optique..

Batterie

Endommagement de la lame

Une installation inadéquate de la batterie peut causer un risque d'explosion ou d'endommagement de la lame.

Utilisez toujours le même type de batterie au lithium tel qu'installé et assurez-vous que la batterie soit installée tel que décrit dans le manuel.

Perte de données

L'installation d'un autre type de batterie que celle montée à la livraison du produit peut causer une perte de données.

Endommagement du PCB ou du support de batterie

N'utilisez pas de tournevis pour retirer la batterie de son support. Retirer la batterie avec un tournevis peut endommager le PCB ou le support de batterie.

Environnement

Dommage Environnemental

Une disposition impropre des produits usagés peut être nocif pour l'environnement.

Éliminez les produits usagés toujours conformément à la législation de votre pays et aux instructions du fabricant.

Sicherheitshinweise

Dieses Kapitel enthält Hinweise, die potentiell gefährlichen Prozeduren innerhalb dieses Handbuchs vorrangestellt sind. Beachten Sie unbedingt in allen Phasen des Betriebs, der Wartung und der Reparatur des Systems die Anweisungen, die diesen Hinweisen enthalten sind. Sie sollten außerdem alle anderen Vorsichtsmaßnahmen treffen, die für den Betrieb des Systems innerhalb Ihrer Betriebsumgebung notwendig sind. Wenn Sie diese Vorsichtsmaßnahmen oder Sicherheitshinweise, die an anderer Stelle diese Handbuchs enthalten sind, nicht beachten, kann das Verletzungen oder Schäden am System zur Folge haben.

Penguin Solutions™ (ist darauf bedacht, alle notwendigen Informationen zum Einbau und zum Umgang mit dem System in diesem Handbuch bereit zu stellen. Da es sich jedoch bei dem System um ein komplexes Produkt mit vielfältigen Einsatzmöglichkeiten handelt, können wir die Vollständigkeit der im Handbuch enthaltenen Informationen nicht garantieren. Falls Sie weitere Informationen benötigen sollten, wenden Sie sich bitte an die für Sie zuständige Geschäftsstelle von Penguin Solutions

Das Produkt wurde so entwickelt, dass es die Anforderungen für die von der Industrie geforderten Sicherheitsvorschriften erfüllt. Es darf nicht in sicherheitskritischen Komponenten, lebenserhaltenden Geräten oder in Flugzeugen verwendet werden.

Einbau, Wartung und Betrieb dürfen nur von durch Penguin Solutions ausgebildetem oder im Bereich Elektronik oder Elektrotechnik qualifiziertem Personal durchgeführt werden. Die in diesem Handbuch enthaltenen Informationen dienen ausschließlich dazu, das Wissen von Fachpersonal zu ergänzen, können dieses jedoch nicht ersetzen.

Halten Sie sich von stromführenden Leitungen innerhalb des Systems fern. Entfernen Sie auf keinen Fall die Systemabdeckung. Nur werksseitig zugelassenes Wartungspersonal oder anderweitig qualifiziertes Wartungspersonal darf die Systemabdeckung entfernen, um Systemkomponenten zu ersetzen oder andere Anpassungen vorzunehmen.

Installieren Sie keine Ersatzteile oder führen Sie keine unerlaubten Veränderungen am System durch, sonst verfällt die Garantie. Wenden Sie sich für Wartung oder Reparatur bitte an die für Sie zuständige Geschäftsstelle von Penguin Solutions. So stellen Sie sicher, dass alle sicherheitsrelevanten Aspekte beachtet werden.

EMV

Das Produkt wurde in einem Penguin Edge™ Standardsystem getestet. Es erfüllt die für digitale Geräte der Klasse A gültigen Grenzwerte in einem solchen System gemäß den FCC-Richtlinien Abschnitt 15 bzw. EN 55022 Klasse A.Diese Grenzwerte sollen einen angemessenen Schutz vor Störstrahlung beim Betrieb des Produktes in einer gewerblichen, geschäftlichen oder industriellen Umgebung gewährleisten.Das Produkt leitet, strahlt und verwendet Hochfrequenzenergie und kann, wenn es nicht ordnungsgemäß installiert und in Übereinstimmung mit dieser Bediehnungsanweisung verwendet wird, schädliche Störungen des Funkverkehrs verursachen.

Der Betrieb des Produkts in einem Wohnbereich verursacht wahrscheinlich schädliche Interferenzen. In diesem Fall muss der Benutzer die Störung auf seine Kosten beheben. Änderungen oder Modifikationen, die nicht ausdrücklich von Penguin Solutions genehmigt wurden, können einzuhaltene Normen oder Vorschriften verletzen. Board Produkte werden in einem repräsentativen System getestet, um die Einhaltung der oben genannten Anforderungen zu gewährleisten. Um die Leistungsfähigkeit zu erhalten is eine ordungsgemäße Installation in einem konformen System erforderlich.

Um sicherzustellen, dass die entsprechenden Vorschriften für die Funkfrequenzen einghalten werden, verwenden Sie beim Anschließen von Peripheriegeräten nur abgeschirmte Kabel. Zur ordnungsgemäßen EMV-Abschirmung, ist das System nur mit installierten Frontblenden zu betreiben und alle freien Steckplätze sind abzudecken oder mit Steckkarten zu fuellen.

Die COM, ETH1, ETH2, USB1, USB2 Schnittstelle(n) sind als Wartungsanschlüsse zu betrachten. Während des Normalbetriebs sollte an diesen Schnittstellen kein Kabel angeschlossen sein. Im Wartungsfall dürfen die angeschlossene Kabel eine Länge von 10 Fuß (3m) nicht überschreiten.

VCCI

Dies ist ein Klasse A Produkt, basierend auf dem Standard des „Voluntary Control Council for Interference” (VCCI) von der „Information Technology Interference”. Wenn dieses Gerät in einem häuslichen Umfeld verwendet wird, können Funkstörungen auftreten. Wenn solche Probleme auftreten, muss der Benutzer möglicherweise Korrekturmaßnahmen ergreifen.

Erdung

Wenn das Produkt nicht richtig geerdet ist, kann es es durch elektrostatische Entladungen beschädigt werden.

Das System enthält EMI-Dichtungen sowohl am System als auch an den einzelnen Modulen. Stellen Sie sicher, dass alle Systemteile die EMV-Dichtung berühren.

Am System befinden sich auch ESD-Kontakte fuer ESD-Bändern. Stellen Sie sicher, dass jede Person, die mit dem System arbeitet, diese als ESD-Schutz benutzt.

Installation

Verletzungsgefahr

Dieses Produkt wird mit gefährlichen Spannungen betrieben, die zu Verletzungen und Tod führen können. Seien Sie äußerst vorsichtig, wenn Sie dieses Gerät und seine Komponenten handhaben, testen und einstellen.

Beschädigung von Schaltkreise

Elektrostatische Entladungen und falsche Installation und Entfernung des Produkts können die Schaltkreise beschädigen oder ihre Lebensdauer verkürzen.

Bevor Sie das Produkt, vergewissern Sie sich, dass Sie in einem ESD-geschützten Bereich arbeiten. Fassen Sie das Produkt nur an den Kanten an und berühren Sie keine Komponenten oder Schaltkreise.

Datenverlust

Warten Sie bis die blaue LED durchgehend leuchtet, bevor Sie das bord herausziehen. Es wird Datenverlust geben, wenn das Bord aus dem System gezogen wird und die blaue LED blinkt noch.

Bereich mit eingeschränktem Zugang

Installieren Sie das Board in ein System nur in Bereichen mit eingeschränktem Zugang.

Beschädigung des Blade und der Zusatzmodule

Lesen Sie daher vor der Installation von Zusatzmodulen die zugehörige Dokumentation.

Fehlerhafte Installation von Zusatzmodulen, kann zur Beschädigung des Blades und der Zusatzmodule führen.

Beschädigung des Blades

Fehlerhafte Installation des Blades kann zu einer Beschädigung des Blades führen.

Verwenden Sie die Handles, um das Blade zu installieren/deinstallieren. Auf diese Weise vermeiden Sie, dass die Frontblende oder die Platine deformiert oder zerstört werden.

Beschädigung des Blades, der Backplane oder von System Komponenten

Verbogene Pins oder lose Komponenten können zu einer Beschädigung des Blades, der Backplane oder von Systemkomponenten führen. Überprüfen Sie das Blades und die Rückwandplatine vor der Installation sorgfältig auf Pin- und Komponentenintegrität.

Penguin Solutions und unsere Zulieferer unternehmen größte Anstrengungen um sicherzustellen, dass sich Pins und Stecker von Blades vor dem Verlassen der Produktionsstätte in einwandfreiem Zustand befinden. Verbogene Pins, verursacht durch fehlerhafte Installation oder durch Installation von Blades mit beschädigten Steckern kann die durch gewährte Garantie für Blades und Backplanes erlöschen lassen.

Beschädigung des Blades

Fehlerhafte Installation des Blades kann zu einer Beschädigung des Blades führen.

Verwenden Sie die Handles, um das Blade zu installieren/deinstallieren. Auf diese Weise vermeiden Sie, dass die Frontblende oder die Platine deformiert oder zerstört werden.

Beschädigung des Blades, der Backplane oder von System Komponenten

Verbogene Pins oder lose Komponenten können zu einer Beschädigung des Blades, der Backplane oder von Systemkomponenten führen. Überprüfen Sie das Blades und die Rückwandplatine vor der Installation sorgfältig auf Pin- und Komponentenintegrität.

Penguin Solutions und unsere Zulieferer unternehmen größte Anstrengungen um sicherzustellen, dass sich Pins und Stecker von Blades vor dem Verlassen der Produktionsstätte in einwandfreiem Zustand befinden. Verbogene Pins, verursacht durch fehlerhafte Installation oder durch Installation von Blades mit beschädigten Steckern kann die durch gewährte Garantie für Blades und Backplanes erlöschen lassen.

Beschädigung des Systems

WARNUG: Die Gebäude-internen Schnittstellen ("intra-building ports" per GR-1089-CORE) der Geräte oder Baugruppen sind nur für gebäudeinterne Verkabelung vorgesehen. Die Schnittstellen sind als Typ 2 oder Typ 4 definiert (wie in GR-1089-Core beschrieben) und erfordern eine Isolation zu Leitungen außerhalb des Gebäudes. Die Gebäude-internen Schnittstellen dürfen keine elektrisch leitende Verbindung zu Leitungen außerhalb des Gebäudes haben. Ein "Primary Protector" (wie in GR-1089-CORE beschrieben) ist keine ausreichende Absicherung, um die Gebäude-internen Schnittstellen mit Leitungen außerhalb des Gebäudes zu verbinden.

Die Gebäude-internen Schnittstellen ("intra-building ports" per GR-1089-CORE) der Geräte oder Baugruppen müssen abgeschirmte Gebäude-interne Verkabelungen verwenden, die an beiden Enden geerdet ist.

RTMs

Beschädigung des RTMs

Fehlerhafte Installation des RTMs kann zu einer Beschädigung des RTMs führen.

Verwenden Sie die Handles, um das RTM zu installieren/deinstallieren. Auf diese Weise vermeiden Sie, dass die Frontblende oder die Platine deformiert oder zerstört werden.

Beschädigung des RTMs, der Backplane oder von System Komponenten

Verbogene Pins oder lose Komponenten können zu einer Beschädigung des RTMs, der Backplane oder von Systemkomponenten führen. Überprüfen Sie das RTM und die Rückwandplatine vor der Installation sorgfältig auf Pin- und Komponentenintegrität.

Penguin Solutionsund unsere Zulieferer unternehmen größte Anstrengungen um sicherzustellen, dass sich Pins und Stecker von Blades/RTMs vor dem Verlassen der Produktionsstätte in einwandfreiem Zustand befinden. Verbogene Pins, verursacht durch fehlerhafte Installation oder durch Installation von Blades/RTMs mit beschädigten Steckern kann die durch gewährte Garantie für Blades und Backplanes erlöschen lassen.

Operation

Stellen Sie sicher, dass die Anzeigegeräte, die dauerhaft an die VGA-Schnittstelle angeschlossen sind, ein Brandgehäuse gemäß den Anforderungen von IEC / EN / UL / CSA 62368-1 und 60950-1 bereitstellen.

Alle anderen Geräte, die nur zu Servicezwecken mit der VGA-Schnittstelle verbunden sind, müssen während des Betriebs überwacht werden und müssen nach den Wartungsarbeiten getrennt werden.

Beschädigung des Produktes - Oberflaeche

Hohe Luftfeuchtigkeit und Kondensat auf der Oberfläche des Produktes können zu Kurzschlüssen führen.

Betreiben Sie das Produkt nicht außerhalb der angegebenen Grenzwerte. Stellen Sie sicher, dass das Produkt vollständig trocken ist und keine Feuchtigkeit auf der Oberfläche ist, bevor Sie den Strom einschalten.

Überhitzung und Beschädigung des Produktes

Stellen Sie beim Betrieb des Produkts sicher, dass das Shelf oder Gehaeuse über eine Zwangsbelüftung verfügt. Betreiben Sie das Produkt ohne Zwangsbelüftung, kann dies zur Überhitzung und Beschädigung des Produktes führen. Wenn das Produkt in Bereichen mit elektromagnetischer Strahlung betrieben wird, sichern Sie das Produkt mit den Schrauben an der Frontblende im System. Stellen Sie sicher, dass das Produkt vollständig vom Gehäuse abgeschirmt ist.

Datenschaden

Wenn die Stromversorgung des Geräts während eines Firmware-Updates des Flash Memory des Geräts unterbrochen wird, werden die Änderungen nicht gespeichert oder der Flash Memory kann beschädigt werden. In diesem Fall bleibt das Produkt wahrscheinlich in einem nicht betriebsbereiten Zustand und muss von qualifizierten Reparaturdiensten überholt werden.

Verletzungen oder Kurzschlüsse — Blade oder Stromversorgung

Falls die OR-ing Dioden des Blades durchbrennen, kann das Blade einen Kurzschluss zwischen den Eingangsleitungen A und B verursachen. In diesem Fall ist Leitung A immer noch unter Spannung, auch wenn sie vom Versorgungskreislauf getrennt ist (und umgekehrt).Um Schäden oder Verletzungen zu vermeiden, überprüfen Sie vor dem Fortsetzen Ihrer Arbeit immer, dass keine Spannung an der Leitung anliegt.

Die Messung der EMV Abstrahlung wurde in einem Referenzsystem mit 10 ATCA-7480 Boards ermittelt, bei denen die "Spread Spectrum" Funktion eingeschalten war. Der Integrator ist dafür verantwortlich, daß seine Konfiguration die EMV Anforderungen erfüllt (z.B. mit einer abweichenden Anzahl von ATCA-7480 Boards oder mit ausgeschalteter "Spread Spectrum" Funktion).

Schaltereinstellungen

Fehlfunktion des Produkt

Ändern Sie nicht die Schaltereinstellungen, die als **Reserved** gekennzeichnet sind. Schalter, die mit **Reserved** gekennzeichnet sind, können produktionsbedingte Funktionen enthalten und zu einer Fehlfunktion des Produktes führen, wenn die Einstellungen geändert werden.

Überprüfen und ändern Sie die Schaltereinstellung, die nicht mit **Reserved** gekennzeichnet sind, bevor Sie das Blade installieren.

Beschädigung des Produkt

Überprüfen und ändern Sie die Schaltereinstellung, bevor Sie das Produkt installieren.

Das Verstellen von Schaltern während des laufenden Betriebes kann zur Beschädigung des Produkt führenn.

Drücken Sie den Reset Schalter nur leicht. Zu viel Druck kann den Reset Schalter beschädigen.

RJ-45 Stecker

Beschädigung des Systems

Bei den RJ-45-Anschlüssen an der Vorderseite handelt es sich entweder um Twisted-Pair-Ethernet- (TPE) oder E1 / T1 / J1-Netzwerkschnittstellen. Wenn Sie eine E1 / T1 / J1-Leitung an einen Ethernet-Anschluss anschließen, kann Ihr System beschädigt werden.

- Kennzeichnen Sie deshalb TPE-Anschlüsse in der Nähe Ihres Arbeitsplatzes deutlich als Netzwerkanschlüsse.
- Stellen Sie sicher, dass die Länge eines Ethernet Kabels, das mit Ihrem System verbundenen ist, 100 m oder 328 feet nicht überschreitet.
- Stellen Sie sicher, dass der TPE-Anschluss des Systems nur mit einem Sicherheits-Kleinspannungs- Stromkreis (SELV - Safety Extra Low Voltage) verbunden werden.
- Bei Fragen wenden Sie sich an Ihren Systemverwalter.

Weitere Informationen finden Sie in der Dokumentation des jeweiligen Produkt.

Hot Swap

Datenverlust

Warten Sie bis die blaue LED durchgehend leuchtet, bevor Sie das bord herausziehen. Es wird Datenverlust geben, wenn das Bord aus dem System gezogen wird und die blaue LED blinkt noch.

Laser

Verletzungsgefahr

Wenn ein Etikett mit der Aufschrift CLASS 1 LASER PRODUCT auf Ihrem System angebracht ist, ist das Gerät mit einem Lasergerät ausgestattet. Diese Geräte enthalten ein Lasersystem, das sichtbare oder unsichtbare Laserstrahlung (oder beides) erzeugt und für die Augen schädlich sein kann.

Suchen Sie zusätzliche Informationen (Leistung, Wellenlänge, Sichtbarkeit, Impulsdauer, anwendbare Normen), bevor Sie Geräte warten. Blicken Sie niemals mit einem optischen Gerät auf das Lasergeräte.

Batterie

Beschädigung des Blades

Unsachgemäßer Einbau der Batterie kann gefährliche Explosionen und Beschädigungen des Blades zur Folge haben.

Verwenden Sie deshalb nur den Batterietyp, der auch bereits eingesetzt wurde und befolgen Sie die Installationsanleitung.

Datenverlust

Wenn Sie einen anderen Batterietyp installieren als den, der bei Lieferung des Produkts montiert wurde, kann dies zu Datenverlust führen.

Beschädigung des PCBs und der Batteriehalterung

Benutzen Sie keinesfalls einen Schraubenzieher, um die Batterie aus der Halterung zu nehmen. Wenn Sie die Batterie mit einem Schraubenzieher ausbauen, können das PCB und die Batteriehalterung beschädigt werden.

Umweltschutz

Umweltschäden

Unsachgemäße Entsorgung von gebrauchten Produkten kann die Umwelt schädigen.

Entsorgen Sie gebrauchte Produkte stets gemäß der in Ihrem Land gültigen Gesetzgebung und den Empfehlungen des Herstellers.

Introduction

1.1 Overview

The Penguin Edge™ ATCA-7480 is a high-performance ATCA compliant single board computer designed for demanding storage and processing applications.

The ruggedized configuration of the ATCA-7480 and is electrically identical to the non-ruggedized ATCA-7480 blade. It features a specially designed alignment block that enables the blade to be secured in a ruggedized AXP1440 chassis which includes special screws in the chassis to securely hold the ruggedized ATCA-7480 to the backplane for rugged environments. Specific information for the ruggedized configuration of the ATCA-7480 can be found in *Appendix A, Ruggedized ATCA-7480 Information on page 323*.

SMART Embedded Computing company branding has changed to Penguin Solutions™. The SMART Embedded Computing product line has been rebranded as Penguin Edge™. No changes were made to the ATCA-7480 product line through this rebranding of the company and product line in April of 2022.

1.2 Features

The main features of the ATCA-7480 board are as follows:

- Designed for NEBS level 3
- Dual socket Intel® Xeon® E5-2600 V3 (Haswell-EP socket LGA2011-3)
- Standard ATCA-7480 configuration:
  - Intel Xeon E5-2648L V3 12-cores 1.8GHz 75W
  - Intel Xeon E5-2618L V3 8-cores 2.3GHz 75W (optional)
  - Intel Xeon E5-2658 V3 12-cores 2.2GHz 105W (optional)
  - DDR4 memory support up to 2133MT/s
  - Four independent DDR4 memory channels per CPU with two DIMM slots per channel (2 DPC) resulting in a total of 16 DIMM slots
  - 8GB and 16GB DDR4 modules in Very Low Profile (VLP) available
- Single slot ATCA form factor (280mm x 322mm)
- Direct CPU to PCIe interface providing 40 PCIe Gen3 lanes (8Gbps)
- Next Generation Communications Platform from Intel, codename Grantley with on-board Intel C612 Wellsburg Platform Controller Hub (PCH)
- Dual Gigabit Ethernet AdvancedTCA Base Interfaces according to PICMG 3.0 based on Intel i350 Powerville

- Quad 40GBASE-KR4,10GBASE-KR,10GBASE-KX4,1000Base-KX: Option1, 1-K,1-KR,9,9-K,9-KR Ethernet AdvancedTCA Fabric Interfaces according to PICMG 3.1 based on Intel XL710 Fortville
- Dual Gigabit Ethernet ports on face plate (Intel i350 Powerville)
- Serial over LAN via AdvancedTCA base Interface
- CPU and I/O virtualization support
- Power management support
- Crisis recovery for BIOS, IPMC Firmware, and FPGA code
- MO297/SlimSATA module carrier slot to carry up to three MO297 type SSD module drives

1.3 Standard Compliances

The product is designed to meet the following standards.

Table 1-1 Standard Compliances

Standard	Description
UL 62368-1 and 60950-1 EN 62368-1 and 60950-1 IEC 62368-1 and 60950-1 UL/CSA 62368-1 and 60950-1	Legal safety requirements
CISPR 22:2008 CISPR 24:2010 EN 55022:2010 EN 55024 FCC Part 15 Subpart B EN 300386 EN 61000-6-2:2005 NEBS Standard GR-1089 Core	Electromagnetic Compatibility (EMC) requirements on system level (predefined Penguin Edge system)
NEBS Standard GR-63-CORE ETSI EN 300019 series	NEBS level three Product is designed to support NEBS level three. The compliance tests must be done with the customer target system.
Directive (EU) 2015/863 (amending Annex II to Directive 2011/65/EU)	Directive on the restriction of the use of certain hazardous substances in electrical and electronic equipment (RoHS)
PICMG 3.0 and 3.1	Defines mechanics, blade dimensions, power distribution, power and data connectors, and system management.

1.4 Mechanical Data

The following table provides details about the mechanical data of the blade.

Table 1-2 Mechanical Data

Feature	Value
Height	322.25mm +0/-0.3mm
Length	280mm +0/-0.3mm
Thickness	2.4mm + 0.2mm
Mounting height top side (component side 1)	21.33mm
Mounting height bottom side (component side 2)	1.61mm
Weight	ATCA-7480-0GB (-L): 3.5kg ATCA-7480-0GB-H: 3.6kg

1.5 Ordering and Support Information

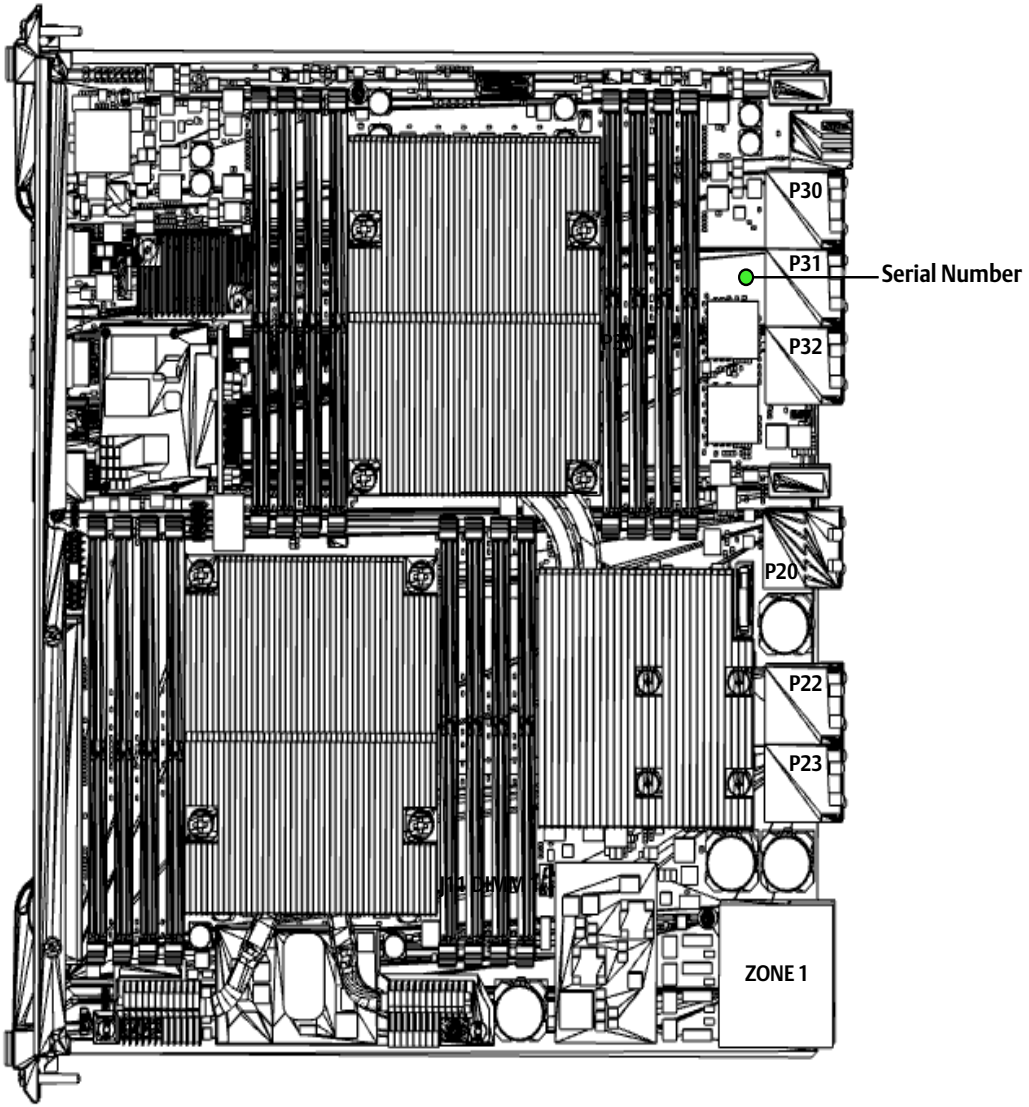
Please reference the data sheet for the Penguin Edge ATCA-7480 blade variants and blade accessories available. Please refer to *Appendix B, Related Documentation on page 327* or consult your local Penguin Solutions sales representative for the availability of other variants.

For technical assistance, documentation, or to report product damage or shortages, contact your local Penguin Solutions sales representative or visit *https://www.penguinsolutions.com/edge/support/.*

1.6 Product Identification

The following figure shows the location of the serial number label.

Figure 1-1 Serial Number Location



Hardware Preparation and Installation

2.1 Unpacking and Inspecting the Blade

NOTICE

Damage of Circuits

Electrostatic discharge and incorrect blade installation and removal can damage circuits or shorten their life.

Before touching the blade or electronic components, make sure that you are working in an ESD-safe environment.

Shipment Inspection

To inspect the shipment, perform the following steps.

1. Verify that you have received all items of your shipment:
   - One ATCA-7480 Series blade
   - One printed copy of *Quick Start Guide*
   - One printed copy of *Safety Notes Summary*
   - Any optional items ordered
2. Check your shipment and report any damage or differences to the Contact Center at *https://www.penguinsolutions.com/edge/support/*.
3. Remove the desiccant bag shipped together with the blade and dispose of it according to your country's legislation.

NOTE: The blade is thoroughly inspected before shipment. If any damage has occurred during transportation or any items are missing, please report via the Contact Center at *https://www.penguinsolutions.com/edge/support/*.

2.2 Environmental and Power Requirements

In order to meet the environmental requirements, the blade has to be tested in the system in which it is to be installed.

Before you power up the blade, calculate the power needed according to your combination of blade upgrades and accessories.

2.2.1 Environmental Requirements

The environmental conditions must be tested and proven in the shelf configuration used. The conditions refer to the surrounding of the blade within the user environment. The product supports the specified temperature conditions in a shelf with the airflow characteristics meeting at least the **CP-TA B.4** cooling profile.

The environmental requirements of the blade may be further limited down due to installed accessories, such as hard disks or mezzanine modules, with more restrictive environmental requirements.

Operating temperatures refer to the temperature of the air circulating around the blade and not to the actual component temperature.

NOTICE

Blade Damage - Blade Surface

High humidity and condensation on the blade surface causes short circuits.

Do not operate the blade outside the specified environmental limits. Make sure the blade is completely dry and there is no moisture on any surface before applying power.

Blade Overheating and Blade Damage

Operating the blade without forced air cooling may lead to blade overheating and thus blade damage.

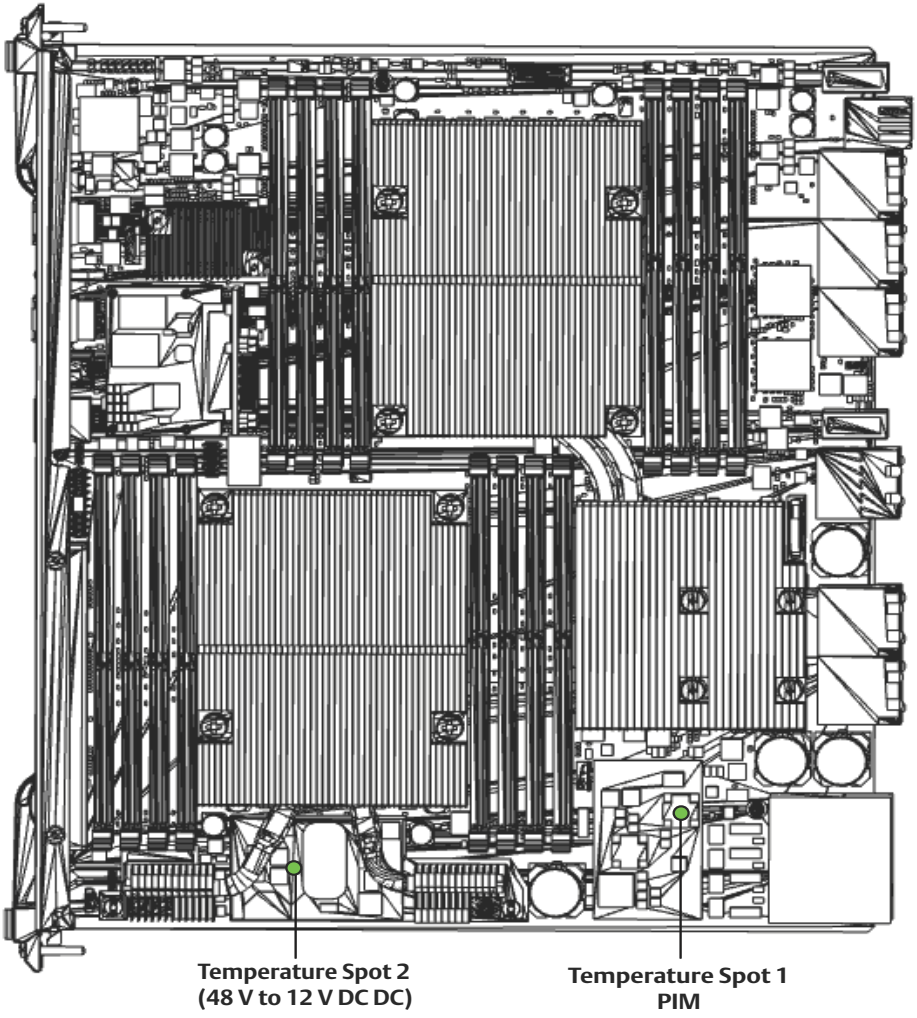
When operating the blade, make sure that forced air cooling is available in the shelf.

Table 2-1 Environmental Requirements

Requirement	Operating	Non-Operating
Temperature	Normal Operation: +5°C (41°F) to +40°C (104°F) according to Telcordia GR-63-CORE (NEBS) and ETSI EN 300 019-1-3, Class 3.1 Exceptional Operation: -5°C (23°F) to +55°C (131°F) according to Telcordia GR-63-CORE (NEBS) Note: This exceeds ETSI EN 300 019-1-3, Class 3.1E requirements (-5°C to +45°C)	-40°C (-40°F) to +70°C (158°F) according to Telcordia GR-63-CORE (NEBS) and ETSI EN 300 019-1-2, Class 2.3 Note: This exceeds ETSI EN 300 019-1-1, Class 1.2 requirements (storage from -25°C (-13°F) to +55°C (131°F) Note: This may be further limited by installed accessories.
Temperature Change	±0.25°C/min according to Telcordia GR-63-CORE	±0.25°C/min
Relative Humidity	Normal Operation: 5%rH to 85%rh non-condensing Exceptional Operation: 5%rH to 90%rh non-condensing According to Telcordia GR-63-CORE (NEBS) and EN 300 019-1-3, Classes 3.1 and 3.1E	5% to 95% non-condensing according to Telcordia GR-63-CORE (NEBS) and EN 300 019-1-1, Classes 1.2 and 2.3
Vibration	1g from 5 to 200Hz and back to 5Hz at a rate of 0.25 octave/minute (according to Telcordia GR-63-core)	5-20Hz at $0.01g^2$/Hz (according to Telcordia GR-63-core and ETSI EN 300 019-2-2) 20-200 Hz at -3 dB/octave Hz (according to Telcordia GR-63-core and ETSI EN 300 019-2-2) Random 5-20Hz at $1m^2/s^3$ Random 20-200Hz at $3m^2/s^3$
Free Fall	-	1.2m/ packaged (according to ETSI 300 019-2-2) 100mm unpackaged (according to Telcordia GR-63-core)

During the safety qualification of this blade, the following on-board locations were identified as critical with regards to the maximum temperature during blade operation. To guarantee proper blade operation and to ensure safety, you have to make sure that the temperatures at the locations specified in *Figure 2-1* are not exceeded. If not stated otherwise, the temperatures should be measured by placing a sensor exactly at the given locations.

Figure 2-1 Location of Critical Temperature Spots (Blade Top Side)



Exact locations of critical temperature spots:

On the PIM (U34) (On top of the transformer). Maximum up to 90^{o}C.

On the 48V/12V DC/DC (U35) (on the PCB, next to the transformer). Maximum up to 125°C.

Table 2-2 Critical Temperature Limits

Component	Thermal Design Power	Max Case or Junction Temperature
All product variants using the following processor: Intel® Xeon® E5-2648L V3	75W	Tmax ~87°C (CPU specific and readable in TEMPERATURE_TARGET register)
All product variants using the following processor: Intel Xeon E5-2618L V3	75W	Tmax ~87°C (CPU specific and readable in TEMPERATURE_TARGET register)
All product variants using the following processor: Intel Xeon E5-2658 V3	105W	Tmax ~87°C (CPU specific and readable in TEMPERATURE_TARGET register)

If you integrate the blade into your own system, contact your local sales representative for further safety information.

2.2.2 Power Requirements

The blade's power requirements depend on the installed hardware accessories. If you want to install accessories on the blade, the load of the respective accessory has to be added to that of the blade. In *Table 2-4 on page 58*, you will find typical examples of power requirements with and without accessories installed. For information on the accessories' power requirements, refer to the documentation delivered together with the respective accessory or consult your local Penguin Solutions representative for further details.

The blade must be connected to a TNV-2 or a safety-extra-low-voltage (SELV) circuit. A TNV-2 circuit is a circuit whose normal operating voltages exceed the limits for a SELV circuit under normal operating conditions, and which is not subject to over voltages from telecommunication networks.

Table 2-3 Power Requirements

Characteristic	Value
Rated Voltage Exception in the US and Canada	-48VDC to -60VDC -48VDC
Operating Voltage Exception in the US and Canada	-39VDC to -72VDC -39VDC to -60VDC

The following table provides information about the maximum power consumption of ATCA-7480 all variants equipped with DIMMs, SSDs, and RTM-ATCA-748x-40G including 4x QSFPs. The table also contains power consumption details of the blade without any RTM.

Table 2-4 Power Consumption of ATCA-7480 with and without RTM

Blade Variant	Configuration	Maximum Power Consumption	Typical Power Consumption
ATCA-7480 variant with 75W 12-cores processors and 16 DIMM sockets (ATCA-7480-xGB)	With RTM-ATCA-748x-40G	289W	258W
	Without any RTM	273W	241W
ATCA-7480 variant with 75W 8-cores processors and 16 DIMM sockets (ATCA-7480-xGB-L)	With RTM-ATCA-748x-40G	255W	229W
	Without any RTM	238W	196W
ATCA-7480 variant with 105W 12-cores processors and 8 DIMM sockets (ATCA-7480-xGB-H)	With RTM-ATCA-748x-40G	337W	289W
	Without any RTM	332W	268W

The blade provides two independent power inputs according to the AdvancedTCA Specification. Each input has to be equipped with an additional fuse of maximum 90A located either in the shelf where the blade is installed or the power entry module (PEM).

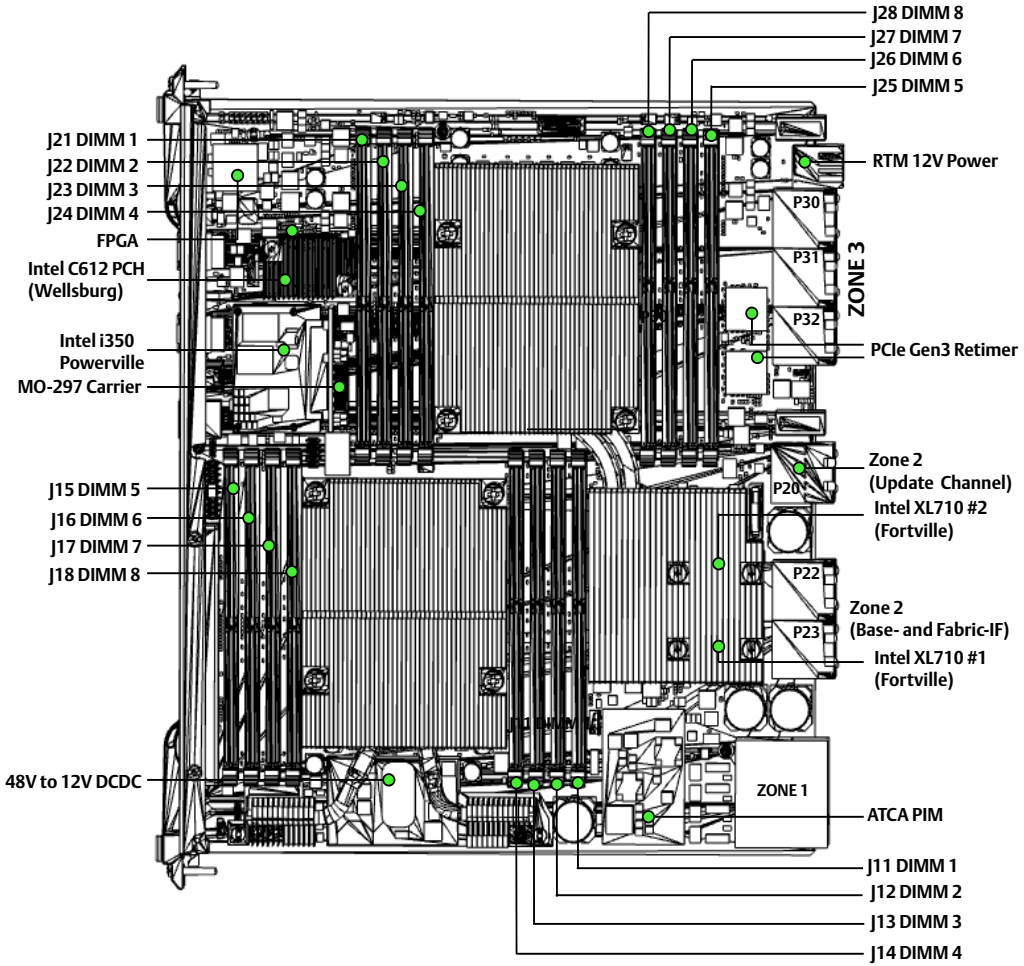
The power consumption has been measured using specific boards in a configuration considered to represent the worst-case (maximum memory population, 3x MO297 SSD modules, with RTM-ATCA-748X-40G and QSFPs) and with software simultaneously exercising as many functions and interfaces as possible. This includes a particular load software provided by Intel designed to stress the processors to reach their theoretical maximum power specification.

Any difference in the system configuration or the software executed by the processors may affect the actual power dissipation. Depending on the actual operating configuration and conditions, customers may see slightly higher power dissipation, or it may even be significantly lower. There is also a dependency on the batch variance of the major components like the processor and DIMMs used. Penguin Solutions does not represent or warrant that measurement results of a specific board provide guaranteed maximum values for a series of boards.

2.3 Blade Layout

The following figure shows the location of components on the ATCA-7480.

Figure 2-2 ATCA-7480 Blade Layout



2.4 Switch Settings

All mechanical switches are OFF in their default configuration. Switch selection used only for debugging are grouped in separate devices, which are not assembled in volume production. Their location is shown in the following figure.

Figure 2-3 Switch Location (Bottom Side of the Blade)

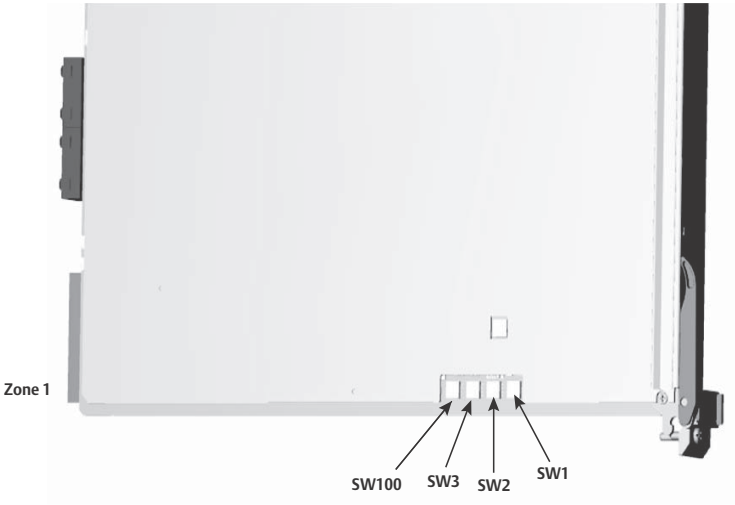


Table 2-5 Switch SW1 settings

Switch	Function	Default	
SW1.1	A2F200 JTAG_SEL strap OFF= JTAG to Fabric (Default) ON= JTAG to CPU-Core	OFF	A2F200 JTAGSEL
SW1.2	BIOS Image Swap	OFF	Default Image ON= Secondary Image in 16MB device
SW1.3	TSOP or Debug-Socket SPI Boot select OFF= Boot from TSOP SPI Flash (either Default/Recovery) ON = Boot from Debug Socket SPI Flash	OFF	Boot from BIOS Socket
SW1.4	Reboot on TCO timeout disabled	OFF	Reboot on TCO disabled

Table 2-6 Switch SW2 Settings

Switch	Function	Default	
SW2.1	Serial Line #1 and #2 Routing OFF=FPGA-COM#1 to face plate FPGA-COM#2 to RTM ON= FPGA-COM#1 to RTM FPGA-COM#2 to face plate	OFF	OFF: COM1 routing to face plate IPMC setting wins always
SW2.2	SW2.2IPMC Debug Console Routing OFF= IPMC Debug Console at 3-pin Header ON= IPMC Debug Console at face plate instead of FPGA COM	OFF	IPMC Debug Console (TTL-level) routing OFF: IPMC Debug Console at 3-pin Header
SW2.3	FPGA_PROM_SEL OFF = 0 (default PROM) ON = 1 (Backup/Recovery PROM)	OFF	Use standard download PROM or redundant download PROM for FPGA configuration
SW2.4	OFF = Reset push button enabled ON = Reset push button disabled	ON	Disable face plate reset push button

Table 2-7 Switch SW3 Settings

Switch	Function	Default	
SW3.1	Manual "Default SPI Boot Flash" / "Recovery SPI Boot Flash" select enable. ON: SW3.2 selects Boot Flash	OFF	IPMI selects Boot Flash
SW3.2	SW3.2 controls Boot flash select if SW3.1 is ON OFF = Boot from “Default SPI Boot Flash” device ON = Boot from “Recovery SPI Boot Flash” device	OFF	OFF = Boot from “Default SPI Boot Flash” device
SW3.3	Debug Output to Serial Console	OFF	No Debug Output to Serial console
SW3.4	Load BIOS defaults	OFF	Do not load BIOS defaults

Table 2-8 Switch SW100 Settings

Switch	Function	Default	
SW100.1	Payload Power Control OFF = Payload power is controlled by IPMC ON = Payload power is forced on and IPMC is disabled	OFF	Payload power is controlled by IPMC
SW100.2	Reserved. Connected to FPGA.	OFF	Reserved
SW100.3	Reserved. Connected to FPGA.	OFF	Reserved
SW100.4	RTM Power Control OFF = RTM power is controlled by IPMC ON = RTM power is forced on	OFF	RTM power is controlled by IPMC

2.5 Installing the Blade Accessories

The following additional components are available for the blade:

- Dual Inline Memory Module (DIMM)
- MO297 SSD Module
- Rear transition modules

They are described in detail in the following sections. For order numbers, refer to the section *Ordering and Support Information on page 51*.

2.5.1 DIMM Memory Modules

The blade provides 16 memory slots for main memory DIMM modules of type DDR4 VLP. You may install and/or remove DIMM memory modules in order to match the main memory size to your needs. The corresponding installation/removal procedures are described in this section.

For the location of the DIMM Memory modules, see *Figure 2-2 on page 59*.

Each processor provides four memory channels with two DIMM sockets each. When installing DIMM memory modules, the DIMM sockets that are farthest away on each memory channel from the CPU device, need to be populated first.

Table 2-9 DIMM Sockets

CPU	Memory channel	DIMM socket	
		Primary	Secondary
CPU#0	A	J11	J12
	B	J13	J14
	C	J15	J16
	D	J17	J18
CPU#1	E	J21	J22
	F	J23	J24
	G	J25	J26
	H	J27	J28

NOTICE

For optimal performance, all memory channels A through H should be populated and also a balanced DIMM configuration is recommended; that is, every memory channel using the same type and amount of DIMMs.

In case of using only one DIMM per channel, make sure that you use only primary sockets and leave the secondary sockets empty.

Only qualified DDR4 DIMMs (Single Ranked or Dual Ranked RDIMM) are allowed; because of the thermal limit/budget of the blade and the high variation of the power consumptions of different DIMM types. For thermal reasons, no 4-rank DIMMs and no dual-Die DIMMs are allowed.

NOTICE

Damage of Circuits

Electrostatic discharge and incorrect module installation and removal can damage circuits or shorten their life.

Before touching the module or electronic components, make sure you are working in an ESD-safe environment.

Installation Procedure

To install a DIMM module, proceed as follows:

1. Remove blade from the system as described in *Installing and Removing the Blade on page 66*.
2. Open the locks of memory module socket.
3. Press the module carefully into socket.
   As soon as the memory module has been fully inserted, the locks automatically close.
4. If applicable, repeat the steps 2 to 3 to install further modules.

NOTICE

Damage of Circuits

Electrostatic discharge and incorrect module installation and removal can damage circuits or shorten their life.

Before touching the module or electronic components, make sure that you are working in an ESD-safe environment.

Removal Procedure

To remove a DIMM module, proceed as follows:

1. Remove the blade from the system as described in *Installing and Removing the Blade on page 66*.
2. Open the locks of socket at both sides. The memory module is automatically lifted up.
3. Remove the module from the socket.
4. Repeat the steps 2 to 3 in order to remove additional memory modules.

2.5.2 SSD Carrier and MO297 SSD Modules

ATCA-7480 provides a modular solution for up to three MO297-A compliant SSDs. Each SSD is connected to the Intel Wellsburg PCH via a SATA interface. The modular approach consists of a riser card, which provide up to three sockets for SSDs and the MO297-A compliant SSDs.

The SSD module is an accessory kit and is not part of the default ATCA-7480. The following procedure describes the steps to install/remove the MO297-A compliant SSD module.

NOTICE

Before mounting the storage on the ATCA-7480, the riser card and SSDs should be pre-mounted.

Installation Procedure

To install an MO297-A SSD module, proceed as follows:

NOTICE

Damage of Circuits

Electrostatic discharge and incorrect module installation and removal can damage circuits or shorten their life.

Before touching the module or electronic components, make sure that you are working in an ESD-safe environment.

1. Remove the blade from the system as described in *Installing and Removing the Blade on page 66*.
2. Plug the SSD module into the MO297-A connector. When inserting the MO297-A module to the on-board connector, hold the on-board connector with two fingers to prevent damage to the connector.
3. Fasten the SSD module to the blade using the screws supplied with the ACC kit.
4. Reinstall the blade into the system as described in *Installing and Removing the Blade on page 66*. The additional resource (either memory or SATA SSD) will be detected automatically during the boot-up sequence.

Removal Procedure

To remove an MO297-A SSD module, proceed as follows:

NOTICE

Damage of Circuits

Electrostatic discharge and incorrect module installation and removal can damage circuits or shorten their life.

Before touching the module or electronic components, make sure that you are working in an ESD-safe environment

1. Remove the blade from the system as described in *Installing and Removing the Blade on page 66*.

2. Remove the two screws holding the SSD module.
3. Remove the SSD module from the blade.
4. Reinstall the blade into the system as described in *Installing and Removing the Blade on page 66*.

2.6 Installing and Removing the Blade

The blade is fully compatible to the AdvancedTCA standard and is designed to be used in AdvancedTCA shelves.

The blade can be installed in any AdvancedTCA node slot. Do not install it in an AdvancedTCA hub slot.

NOTICE

Damage of Circuits

Electrostatic discharge and incorrect blade installation and removal can damage circuits or shorten their life. Before touching the blade or electronic components, make sure that you are working in an ESD-safe environment.

Blade Malfunctioning

Incorrect blade installation and removal can result in blade malfunctioning. When plugging the blade in or removing it, do not press on the face plate but use the handles

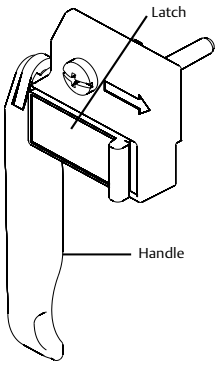
2.6.1 Installing the Blade

The following procedure describes the installation of the blade. It assumes that your system is powered on. If your system is not powered on, you can disregard the blue LED and skip the respective step. In this case, it is purely a mechanical installation.

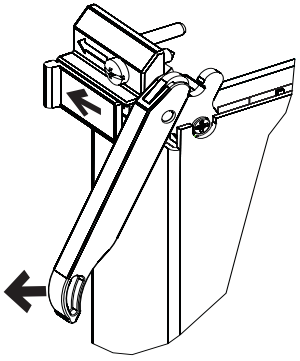
Installation Procedure

To install the blade into an ATCA shelf:

1. Visually inspect the blade and backplane connectors for damage or bent pins before attempting to insert a blade. If any connector damage or pin damage is observed, stop inserting the blade and send the damaged item to proper repair channels.

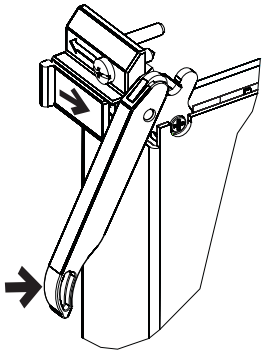


2. Slide the latch into the release position and pull out the handle outward to unlatch the handle from the face plate. Do not rotate the handle fully outward.



3. Insert the blade into the shelf by placing the top and bottom edges of the blade in the card guides of the shelf. Make sure that the guiding module of shelf and blade are aligned properly.
4. Apply equal and steady pressure to the blade to carefully slide the blade into the shelf until you feel resistance. Continue to push the blade gently until the blade connectors engage.

5. Fully insert the blade and turn the handle towards the face plate. The latch automatically slides inwards and locks the handle.



If you feel that you need an abnormal amount of force during blade insertion into the slot, extract the blade, then carefully inspect the blade and slot for problems to prevent damage.

If your shelf is powered, as soon as the blade is connected to the backplane power pins, the blue LED is illuminated.

When the blade is completely installed, the blue LED starts to blink. This indicates that the blade has signified its presence to the shelf management controller.

If an RTM is connected to the front blade, make sure that the handles of both the RTM and the front blade are closed in order to power up the blade's payload.

6. Wait until the blue LED is switched off, then fasten the face plate screws, which secure the blade to the shelf. When the blue LED is switched OFF and the green LED (IS) is switched ON, this indicates that the payload has been powered up and the blade is active.
7. Connect cables to the face plate, if applicable.

2.6.2 Removing the Blade

This section describes how to remove the blade from an AdvancedTCA system.

NOTICE

Damage of Circuits

Electrostatic discharge, incorrect blade installation and removal can damage circuits or shorten their life.

Before touching the blade or electronic components, make sure you are working in an ESD-safe environment.

Blade Malfunctioning

Incorrect blade installation and removal can result in blade malfunctioning.

When plugging the blade in or removing it, do not press on the face plate, instead use the handles.

Removal Procedure

The following procedure describes how to remove the blade from a shelf. It assumes that the system is powered on. If the system is not powered on, you can disregard the blue LED and skip the respective steps. In that case, it is purely a mechanical procedure.

1. Unlatch the handle from the face plate by sliding the latch into the release position and pull out the handle outward. Do not rotate the handle fully outward. The blue LED starts blinking indicates that the blade power-down process is ongoing.
2. Wait until the blue LED is illuminated permanently. Loosen the screws of the face plate, then unlatch the handle and rotate the handle fully outward until the blade is detached from the shelf.

If the LED continues to blink, a possible reason may be that the upper layer software has rejected the blade extraction request.

NOTICE

Data Loss

Removing the blade with the blue LED still blinking causes data loss.

Wait until the blue LED is permanently illuminated before removing the blade.

3. Remove the face plate cables, if applicable.

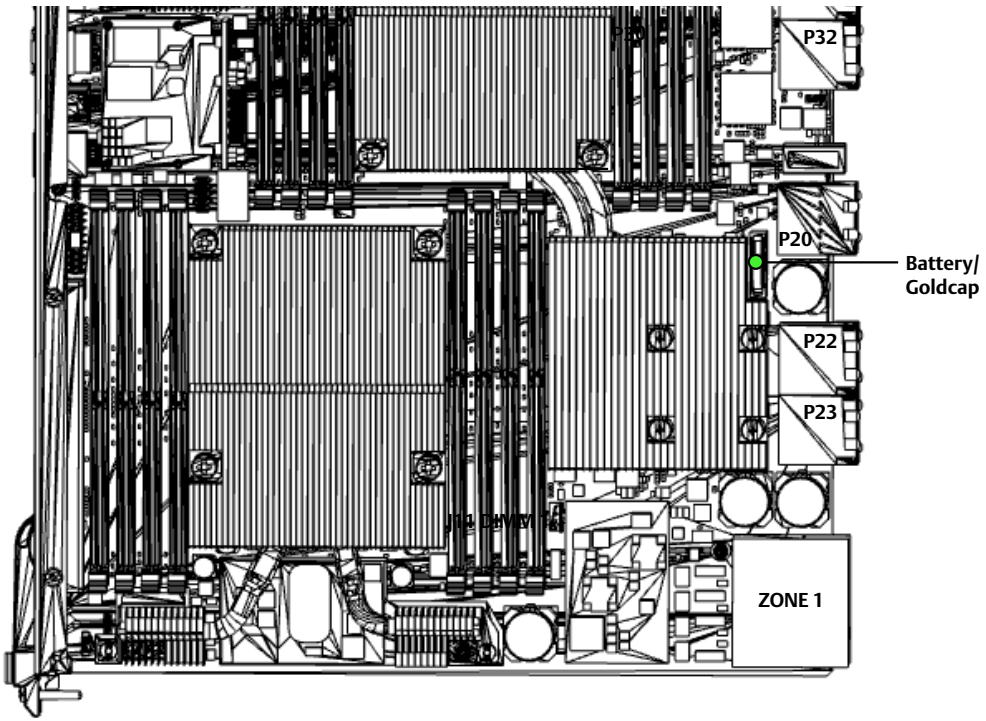
4. Loosen the screws of the face plate until the blade is detached from the shelf.
5. Remove the blade from the shelf.

2.7 Replacing the Battery

Some blade variants contain an on-board battery. Its location is shown in the following figure.

A battery-less variant based on SUPERCAP is available on demand.

Figure 2-4 Location of On-board Battery



The battery provides data retention of seven years summing up all periods of actual data use. Penguin Solutions therefore assumes that there is usually no need to replace the battery except, for example, in case of long-term spare part handling.

NOTICE

Board/System Damage

Incorrect replacement of lithium batteries can result in a hazardous explosion. Replace the battery as described in this chapter.

Data Loss

If the battery does not provide enough power anymore, the RTC is initialized and the data in the NVRAM is lost. Replace the battery before seven years of actual battery use have elapsed.

Replacing the battery always results in data loss of the devices which use the battery as power backup. Back up affected data before replacing the battery.

Installing another battery type other than what is mounted at board delivery may cause data loss. This is because other battery types may be specified for other environments or may have a shorter lifespan. Therefore, only use the same type of lithium battery as is already installed and replace the battery as described in this chapter.

Replacement Procedure

NOTICE

PCB and Battery Holder Damage

Removing the battery with a screw driver may damage the PCB or the battery holder. To prevent this damage, do not use a screw driver to remove the battery from its holder.

To replace the battery:

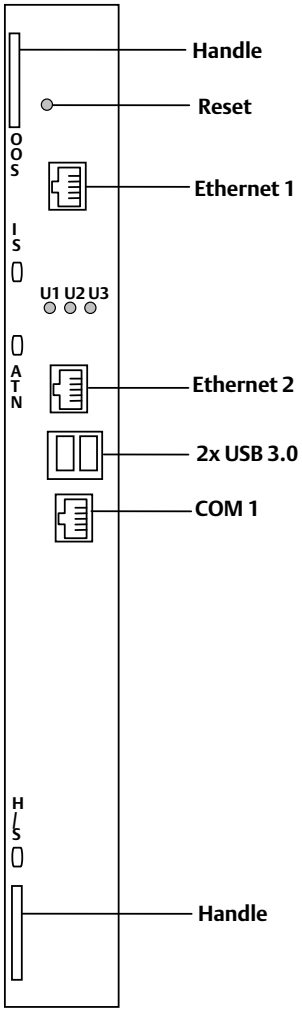
1. Remove battery.
2. Install the new battery following the positive (+) and negative (-) signs.

Controls, Indicators, and Connectors

3.1 Face Plate

The following figure illustrates the connectors, keys, and LEDs available on the ATCA-7480 face plate.

Figure 3-1 Face Plate



3.1.1 LEDs

The LEDs on the face plate are described in the following table.

Table 3-1 Face Plate LEDs

LED	Description
OOS	Out Of Service Red/optional Amber (controllable by IPMC): This LED is controlled by higher layer software, such as middle ware or applications.
IS	Payload Power Status Green: The payload power has been enabled by the IPMC. Note that this LED indicates the payload power status both in the early power state and the normal blade operation. OFF: Payload power is disabled Note: This LED is multicolored (red/green/yellow) and is programmable by IPMC.
ATN	Amber: This LED is controlled by higher layer software, such as middle ware or applications.
ETH Status LEDs	The Ethernet connector provides two status LEDs Link (upper) Green: Link is available Off: No link Activity (lower) Yellow: Activity Off: No activity
U1, U2	Base interface activity is visualized via FPGA LEDs U1 and U2
U3	User LED, selectable color via FPGA register. Colors: Red, Green, Amber
H/S	FRU State Machine During blade installation: Permanently blue: On-board IPMC powers up Blinking blue: Blade communicates with shelf manager OFF: Blade is active During blade removal: Blinking blue: Blade notifies shelf manager of its desire to deactivate Permanently blue: Blade is ready to be extracted

3.1.2 Keys

The blade provides one face plate reset key. On pressing it, a hard reset is triggered and all the attached on-board devices are reset.

You cannot reset the IPMC via this key.

3.1.3 Connectors

The blade provides the following connectors at its face plate:

- 2x Ethernet
- 1x Serial
- 2x USB 3.0/USB 2.0

3.1.3.1 Serial COM#1 P17

Serial line interface #1 of Glue Logic FPGA is available on the ATCA-7480 face plate. A female RJ-45 connector is used for serial line connection. The pinout in the following table is used according to the Cisco-like pinout. The pins which are unconnected are marked as "n.c".

Table 3-2 RJ-45 Female Serial Line Connector Pinout

Pin	Signal
1	n.c
2	n.c
3	COM1_RS232_TXD
4	GND
5	GND
6	COM1_RS232_RXD
7	n.c
8	n.c

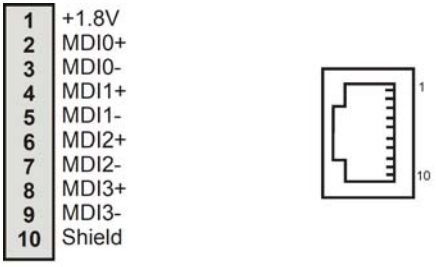
3.1.3.2 Ethernet Connector

There are two Ethernet connectors:

- ETH1 connector P70
- ETH2 connector P71

The pinout of the connector is shown in the following figure.

Figure 3-2 Ethernet Interface Connectors Pinout

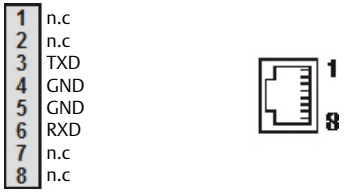


3.1.3.3 Serial Interface Connector

The blade provides one RS-232 serial interface connector at its face plate. It is of type RJ-45 and corresponds to the physical serial interface port 1. By default, the BIOS maps this interface to the serial interface COM1. The on-board switch 2-1 allows to swap COM1 with COM2, making COM2 accessible through the face plate connector instead. The BIOS serial redirection feature uses COM1 as access interface. Therefore, swapping the serial interfaces via SW2-1 also changes the serial connector that you need to access to make use of the serial redirection feature.

The pinout of the serial interface connector is shown below.

Figure 3-3 Serial Interface Connector Pinout

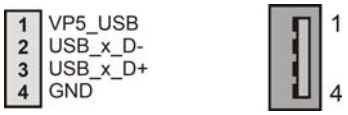


3.1.3.4 USB 3.0 Connectors

The blade provides two USB 3.0 connectors at its face plate and one USB at RTM (zone 3) interface. The USB connectors at face plate are compliant to the USB 3.0 standard and correspond to the blade's USB interfaces 3 and 4. The USB at RTM interface is compliant to USB 2.0.

The pinout of each USB connector is shown in the following figure.

Figure 3-4 USB Connector Pinout



Attaching a device to the front panel USB ports that exceeds the maximum USB current rating of 500mA per port will result in the ATCA-7480 protecting itself through a controlled board shutdown.

3.2 On-board Connectors

The blade provides the MO297 SSD module carrier connector on board.

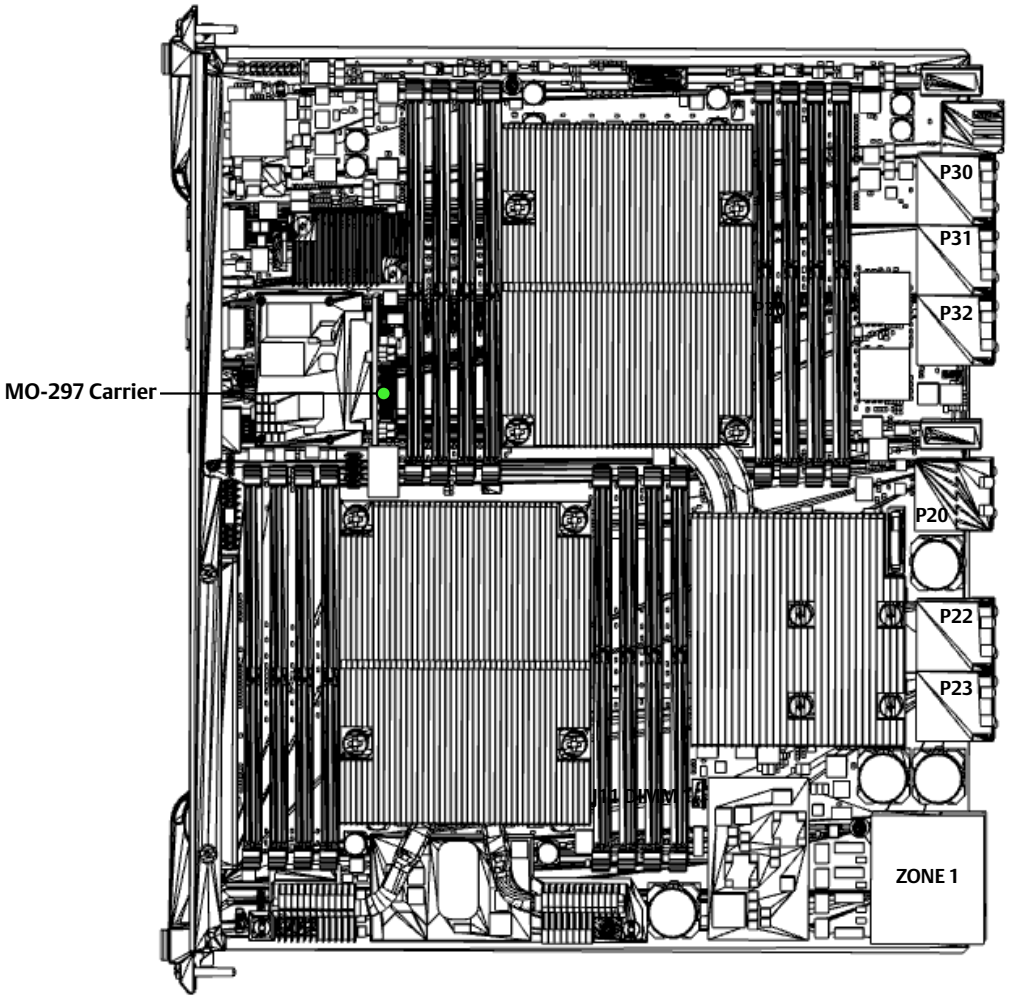
3.2.1 MO297 SSD Module Carrier Connector

The MO297 SSD module Carrier (Riser card) connects three SATA interfaces of the Wellsburg PCH to three slots of standard MO297 type SSD flash discs. This carries the following types of signals:

- 3 SATA port (from PCH)
- Power supply 5V and 3.3V

The location of the MO297 SSD module carrier/riser is illustrated in the following figure.

Figure 3-5 Location of MO297 SSD Module Connector



The pinout of this connector is illustrated in the following figure.

Figure 3-6 MO297 SSD Module Carrier Connector Pinout

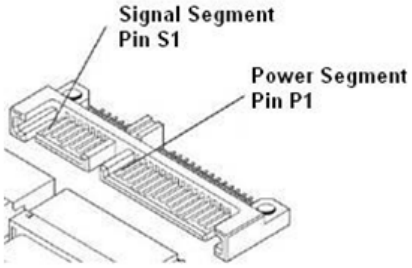


Table 3-3 Signal Segment Pinout

Pin Number	Function	Description
S1	GND	2nd mate
S2	A+	Differential signal Pair A
S3	A-	
S4	GND	2nd mate
S5	B-	Differential signal Pair B
S6	B+	
S7	GND	2nd mate

Table 3-4 Power Segment Pinout

Pin Number	Function
P1	Not used (3.3V)
P2	Not used (3.3V)
P3	Not used (3.3V Pre-Charge)
P4	GND
P5	GND
P6	GND
P7	5V Pre-Charge

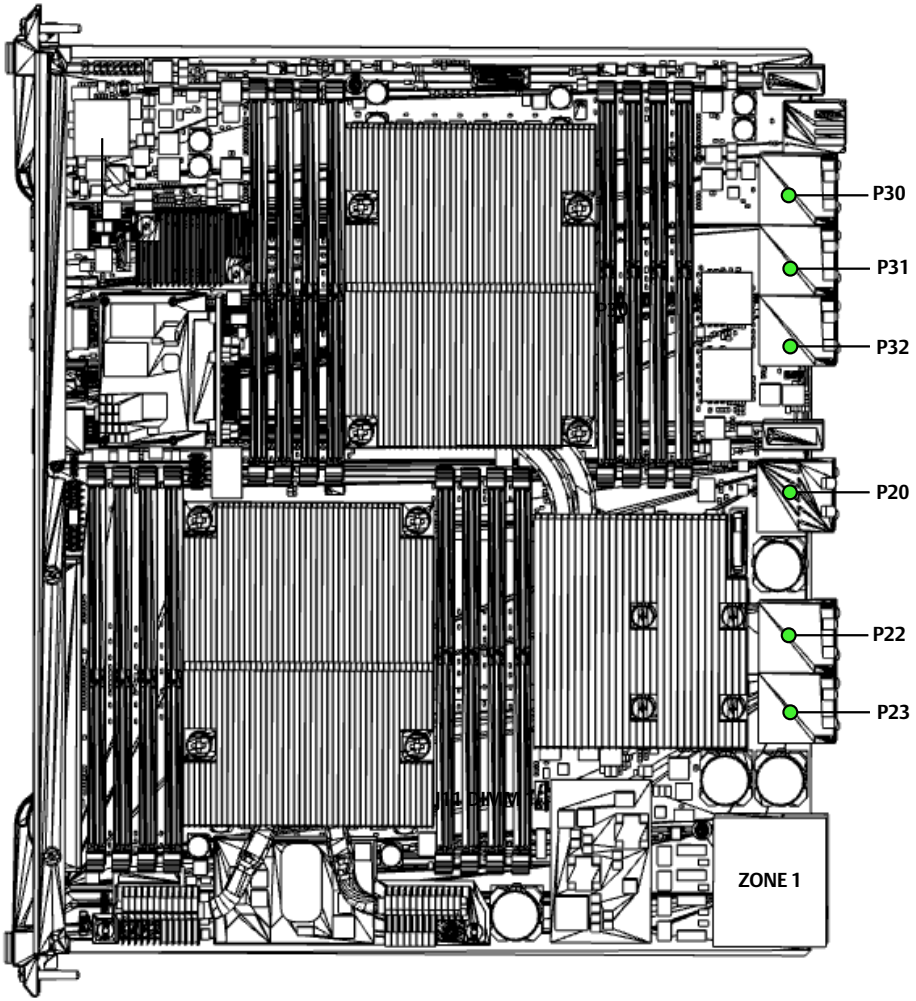
Table 3-4 Power Segment Pinout (continued)

Pin Number	Function
P8	5V
P9	5V
P10	GND
P11	RESERVED
P12	GND
P13	Not used (12V Pre-Charge)
P14	Not used (12V)
P15	Not used (12V)

3.3 AdvancedTCA Backplane Connectors

The AdvancedTCA backplane connectors reside in three Zones 1 to 3 as specified by the AdvancedTCA standard, and are called P10, P20 and P23, P30, P31 and P32. The pinouts of all these connectors are given in this section.

Figure 3-7 Location of AdvancedTCA Connectors

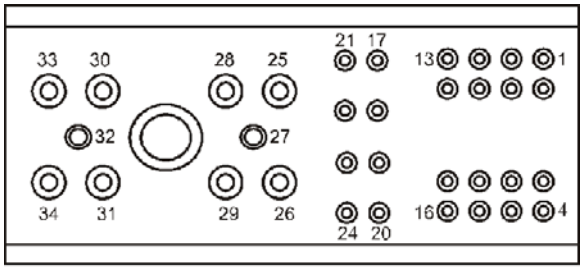


The connector residing in Zone 1 is called P10 and it carries the following signals:

- Power feed for the blade (VM48_x_CON and RTN_x_CON)
- Power enable (ENABLE_x)

- IPMB bus signals (IPMB0_x_yyy)
- Geographic address signals (HAx)
- Ground signals (SHELF_GND and GND)
- Reserved signals

Figure 3-8 P10 Backplane Connector Pinout



1	Reserved	18	n.c.
2	Reserved	19	n.c.
3	Reserved	20	n.c.
4	Reserved	21	n.c.
5	HA0	22	n.c.
6	HA1	23	n.c.
7	HA2	24	n.c.
8	HA3	25	SHELF_GND
9	HA4	26	GND
10	HA5	27	ENABLE_B
11	HA6	28	RTN_A_CON
12	HA7	29	RTN_B_CON
13	IPMB0_A_SCL	30	n.c.
14	IPMB0_A_SDA	31	n.c.
15	IPMB0_B_SCL	32	ENABLE_A
16	IPMB0_B_SDA	33	VM48_A_CON
17	n.c.	34	VM48_B_CON

Zone 2 contains two connectors P20 and P23. They carry the following types of signals:

- Telecom clock signals (CLKx_)
- Base interface signals (BASE_)
- SAS update channel
- 100Base-BX update channel

Some of the pins provided by P20 and P23 are defined as optional in the AdvancedTCA specification and are unused on the blade. If the AdvancedTCA specification defines these signals as input signals, they are terminated on the blade and marked as “TERM_” in the following pinouts. In all other cases the pins are unconnected and consequently marked as "n.c".

The pinouts of P20, P22, P23, P30, P31, and P32 connectors are shown below.

Figure 3-9 P20 Backplane Connector Pinout - Rows A to D

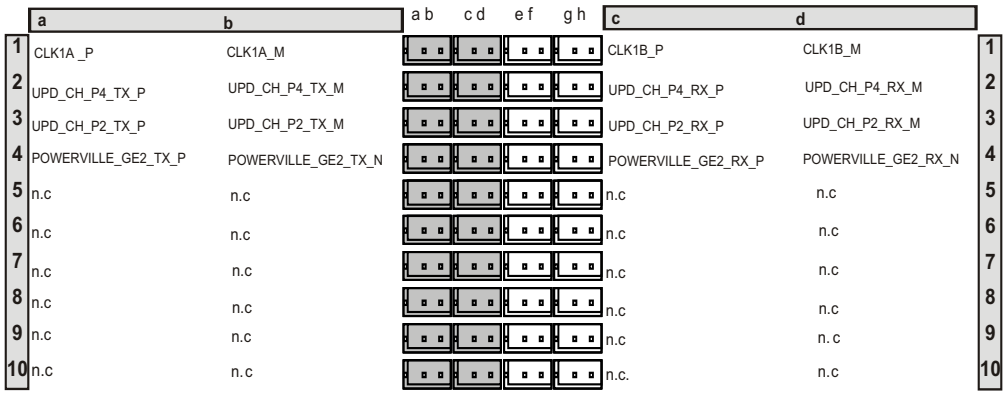


Figure 3-10 P20 Backplane Connector Pinout - Rows E to H

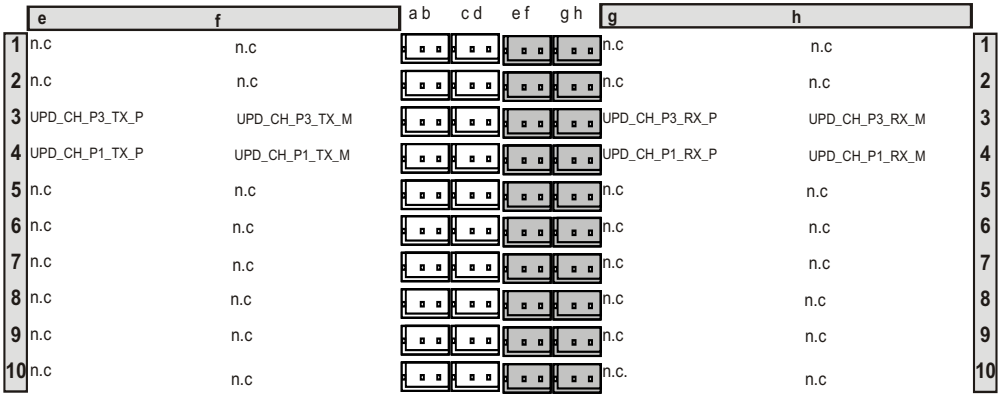


Figure 3-11 P22 Backplane Connector Pinout - Rows A to D

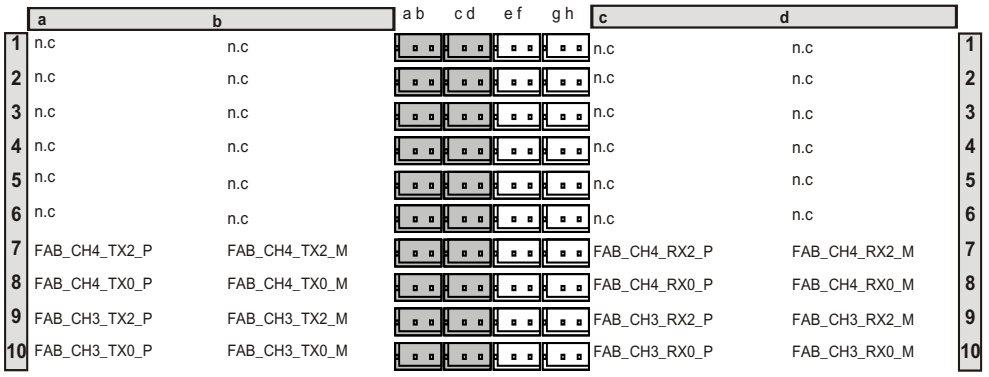


Figure 3-12 P22 Backplane Connector Pinout - Rows E to H

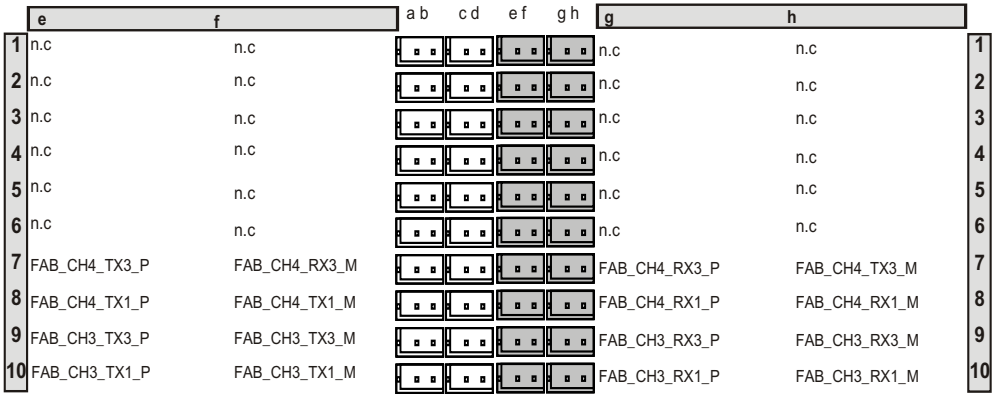


Figure 3-13 P23 Backplane Connector Pinout - Rows A to D

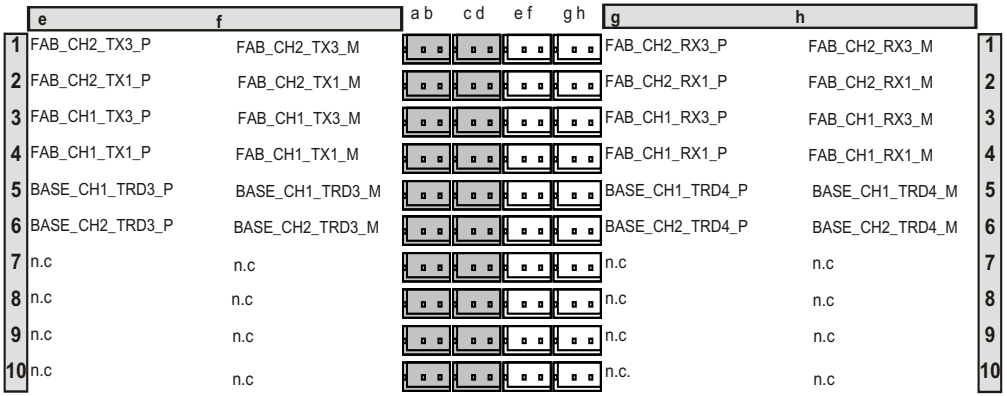
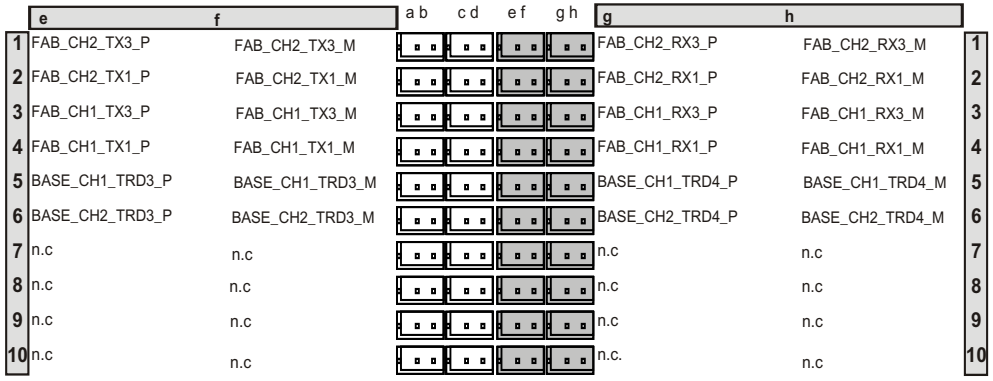


Figure 3-14 P23 Backplane Connector Pinout - Rows E to H



Zone 3 contains the three connectors P30, P31, and P32. They are used to connect an RTM to the blade and carry the following signals:

- Serial (RS232_x_yyyy)
- Serial ATA (SATAx_yyy)
- USB (USBxy)
- PCI Express (PCIEx_yyy)
- IPMI (IPMB1_xxx, ISMB_xxx)
- Power (VP12_RTM, V3P3_RTM, VP5_RTM)
- SAS Update channels
- General control signals (BD_PRESENTx, RTM_PRSNT_N, RTM_RST_KEY-, RTM_RST-)

Figure 3-15 P30 Backplane Connector Pinout - Rows A to D

	a	b	ab cd ef gh	c	d	
1	_88_SERIAL_RTM_RXD	_88_SERIAL_RTM_TXD		JTAG_TDO_5	JTAG_TDI	1
2	SAS2_TX_P	SAS2_TX_M		SAS2_RX_P	SAS2_RX_M	2
3	SAS0_TX_P	SAS0_TX_M		SAS0_RX_P	SAS0_RX_M	3
4	USB_ICH_P8_P	USB_ICH_P8_		n.c	n.c	4
5	n.c	n.c		n.c	n.c	5
6	PCIE_PORT10_RX_P<0>	PCIE_PORT10_RX_M<0>		PCIE_PORT10_RX_P<0>	PCIE_PORT10_RX_M<0>	6
7	PCIE_PORT10_RX_P<2>	PCIE_PORT10_RX_M<2>		PCIE_PORT10_RX_P<2>	PCIE_PORT10_RX_M<2>	7
8	CLK100__RTMPCIE10_P	CLK100_RTMPICE10_M		_88_RTM_PCIE_RST	JTAG_TRST_N	8
9	RTM_IPMB_SCL	RTM_IPMB_SDA		V3P3_MGMT_RTM\G	n.c (Reserved)	9
10	RTM_VP12	RTM_VP12		n.c. (RTM_V3P3)	n.c (RTM_V3P3)	10

Figure 3-16 P30 Backplane Connector Pinout - Rows E to H

	e	f	ab cd ef gh	g	h	
1	n.c	n.c		RTM_PS1_N	RTM_POWERGOOD	1
2	SAS3_TX_P	SAS3_TX_M		SAS3_RX_P	SAS3_RX_M	2
3	SAS1_TX_P	SAS1_TX_M		SAS1_RX_P	SAS1_RX_M	3
4	SATA1_TX_P	SATA1_TX_N		SATA1_RX_P	SATA1_RX_N	4
5	n.c	n.c		n.c	n.c	5
6	PCIE_PORT10_RX_P<1>	PCIE_PORT10_RX_M<1>		PCIE_PORT10_TX_P<1>	PCIE_PORT10_TX_M<1>	6
7	PCIE_PORT10_RX_P<3>	PCIE_PORT10_RX_M<3>		PCIE_PORT10_TX_P<3>	PCIE_PORT10_TX_M<3>	7
8	JTAG_TCK_RTM	JTAG_TMS_RTM		_88_RTM_SHIFT_CLK	_88_RTM_LATCH_CLK	8
9	Reserved	_88_RTM_PS0_N		_88_RTM_RST_KEY_N	_88_RTM_RST_OUT_N	9
10	n.c (RTM_VP5)	RTM_ENABLE_N		_88_RTM_I2C_CLK	_88_RTM_I2C_DAT	10

Figure 3-17 P31 Backplane Connector Pinout - Rows A to D

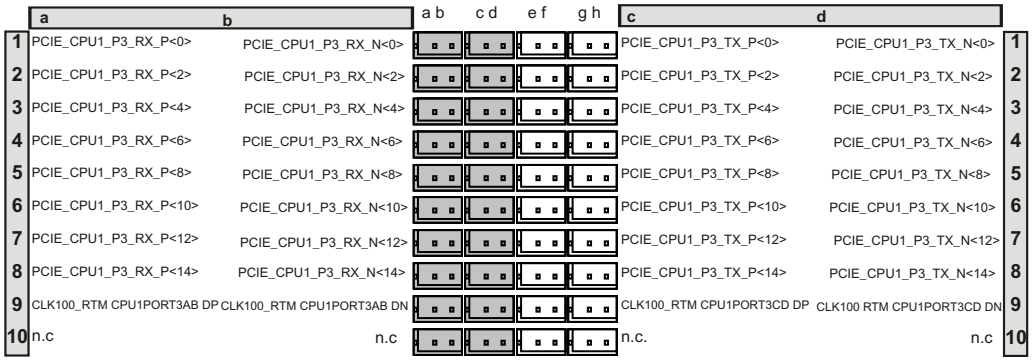


Figure 3-18 P31 Backplane Connector Pinout - Rows E to H

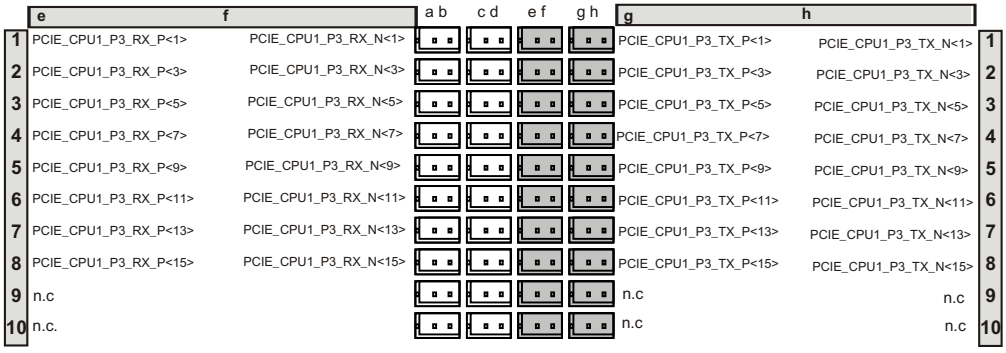


Figure 3-19 P32 Backplane Connector Pinout - Rows A to D

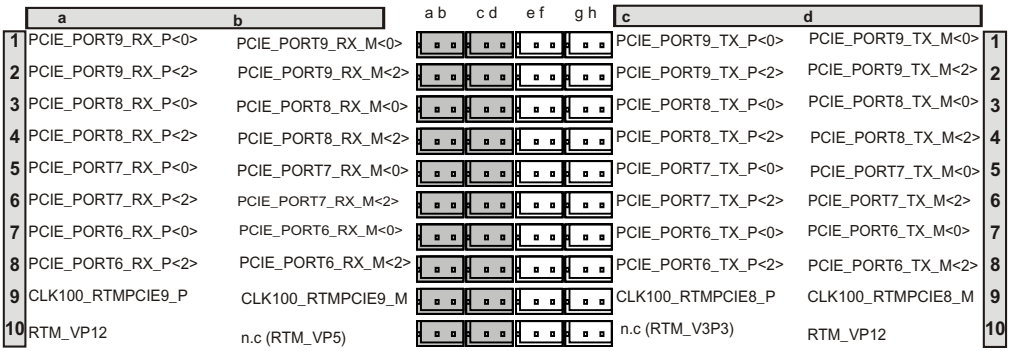
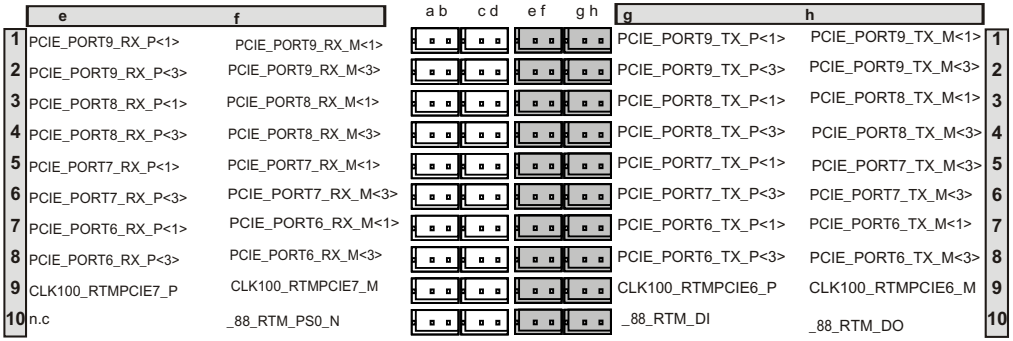


Figure 3-20 P32 Backplane Connector Pinout - Rows E to H

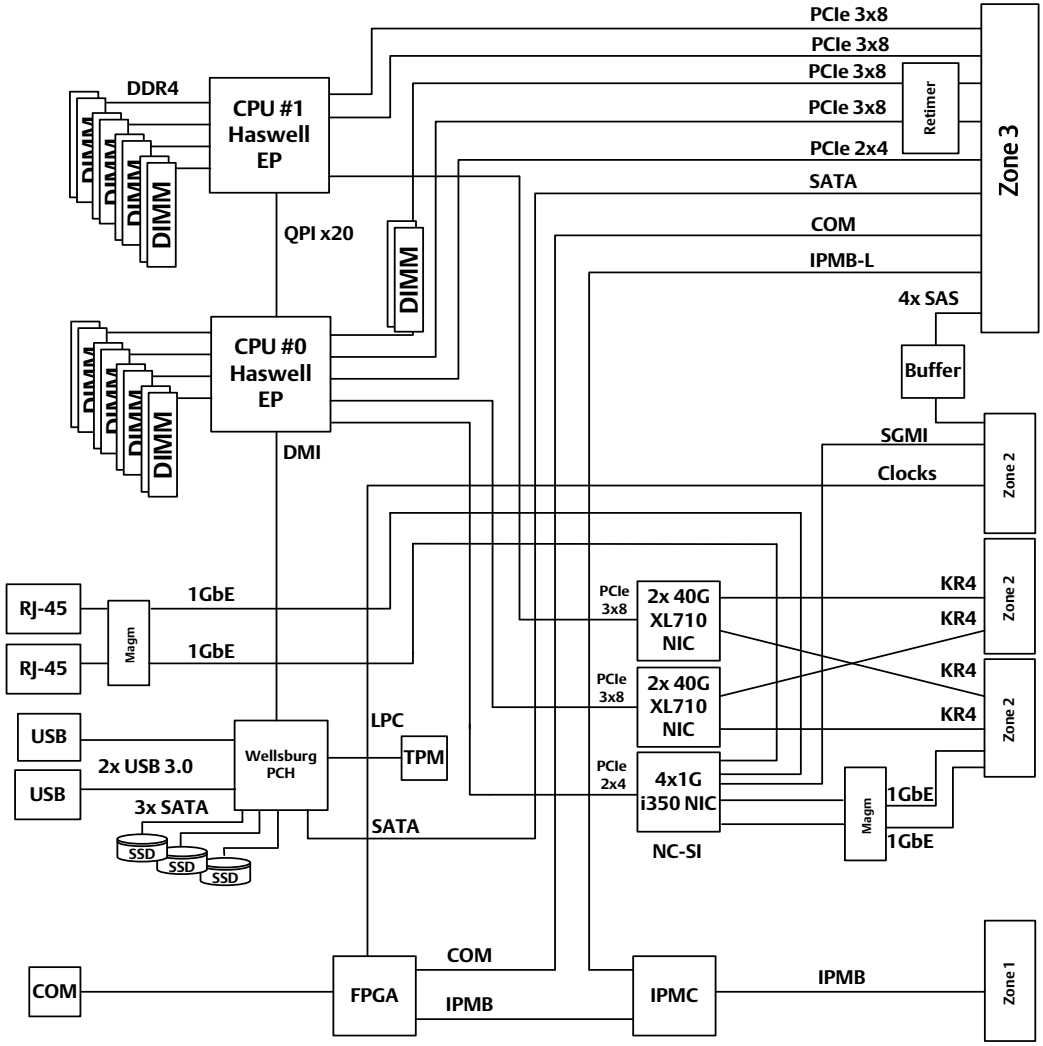


Functional Description

4.1 Block Diagram

The block diagram shows how the devices work together and the data paths used.

Figure 4-1 ATCA-7480 Block Diagram



4.2 Processor

ATCA-7480 provides two Intel Xeon E5-26xxL V3 (Haswell-EP) server processors as the central processing unit (CPU). Each processor provides 40 PCIe lanes up to Gen3 speeds (8GT/s). The processors are connected with each other through two Intel QuickPath Interconnect point-to-point links capable of up to 9.8GT/s. Each processor provides an integrated 4-channel DDR4 Memory Controller (IMC) supporting up to DDR4-2133.

4.3 DDR4 Main Memory

The blade provides two CPUs which has four channels of independent DDR4 memory on each CPU. On each of the eight DDR4 channels the blade provides two DIMMs. The latest JEDEC specification defines a DDR4 socket with 288 pins. Registered DDR4 DIMMs are used for best performance.

The following are the DDR4 module specifications:

- DDR4-2133
- Very Low Profile
- Max two ranks per DIMM
- 8 and 16 GByte capacity
- Standard voltage (1.2V)
- Speed up to DDR4-2133 (PC4-2133) for 1DPC
- Speed up to DDR4-1866 (PC4-1866) for 2DPC

When mixing DIMMs of different speed selections, BIOS set up the lowest speed for all memory channels/DIMM slots on per CPU level basis.

The following are the supported memory features:

- RAS features supported with ECC (Mirroring, x8/x4 SDDC, Sparing, Scrubbing)
- Memory Error signaling for uncorrectable errors
- Memory Error signaling for correctable memory errors
- ADR feature to support persistent memory structures in DDR3 (asynchronous DRAM refresh)

4.4 Platform Controller Hub Intel C612 Wellsburg

The Next Generation Communications Platform Controller Hub (codename Wellsburg) Intel C612 PCH provides access between processors and the I/O subsystem. The PCH connects to CPU#0 through Intel DMI2.0, PCH I/O-controller connected to DMI2 interface of CPU#0.

ATCA-7480 supports Intel Hybrid Clocking Mode through the Intel C612 PCH controller. By default, the Spread Spectrum Clocking (SSC) feature is enabled for the 100MHz CPU and the PCIe clocks, which are provided by the Intel C612 and buffered through DB1900 buffer. If SSC is enabled in BIOS settings, all PCIe devices that are connected on-board or via RTM module will receive SSC clock. SSC can be disabled using BIOS settings.

The SSC tolerance is ±0.25% from nominal frequency (100 MHz).

4.4.1 PCH I/O Controller Features

The following are the PCH I/O Controller features:

- x4 PCIe Gen1 (2.5GT/s) connected to VGA module slot
- 8237 DMA controller
- 8254 based Counter Timer/timers
- 8259 Interrupt Controllers PIC (D31:F0)
- I/O APIC controller (D31:F0)
- Serial Interrupt (D31:F0)
- RTC with 256-byte battery-backed SRAM (D31:F0) (D31:F7)
- Processor Interface (D31:F0) including Thermtrip input and A20GATE, INIT3_3V, CPUPWRGD, PMSYNC#, PECI
- Two stage Watchdog timer (WDT) (D31:F7)
- SPI Interface (Boot Flash)
- LPC/KCS Interface
- Up to 10 serial ATA (SATA) controllers 6Gb/s of which four are used on ATCA-7480
- Six USB 3.0 and 8 PCIe 2.0 interfaces of which 2+2 are used on ATCA-7480
- Power management support (D31:F0) including ACPI S3 state support (suspend to RAM) and Management Engine Power Management support
- High Precision Event Timers (HPET)
- System TCO (total cost of ownership) Reduction circuits
- SMBus Host controller (D31:F3) and SMLINK0,1 interface for communication with external IPMC controller
- General purpose I/O pins (D31:F0)

4.4.2 Firmware Flashes

The blade has two physically separate 16MB flash devices hosting the BIOS firmware.

- Primary (or Default BIOS) Flash (SPI 0)
- Recovery BIOS Flash (SPI 1)

The flash is allocated for storing the binary code of the BIOS. The ATCA-7480 boots from the primary flash SPI 0 under normal circumstances. If booting BIOS from primary flash SPI 0 fails, a hardware mechanism automatically changes the flash device select logic to boot from the recovery flash SPI 1. The image that the processor will boot from after next reset is determined by the IPMC. It can be selected via dedicated IPMI OEM command.

4.5 ATCA Base Interface Ethernet Controller

The i350 four 1Gb Ethernet MACs are used on ATCA-7480 to provide:

- Dual AdvancedTCA Base Interface 10/100/1000Base-T
- Two face plate 10/100/1000Base-T interfaces

On the ATCA-7480, Intel i350 Ethernet controller provides separate interface pins for copper interface (1000Base-T type) and SERDES (1000Base-KX). Four copper interface ports are connected to two face plate and two ATCA Base-IF 1000Base-T interfaces. From the SERDES interfaces only Port 2 is used and connected to the ATCA Zone 2 Update Channel Port 0.

The following table shows the Intel i350 Ethernet port mapping.

Table 4-1 Intel i350 Ethernet Port Mapping

Port #	i350 PHY/Copper Port	i350 SERDES Port
0	ATCA- Base IF#1	NC (Not Connected)
1	ATCA- Base IF#2	NC
2	Face plate #1	ATCA Update Channel Port#0
3	Face plate #2	NC

The selection of which port to use, either the 1000Base-T (copper) port or the SERDES port is controlled through the firmware programmed in the i350 configuration EEPROM.

4.5.1 ATCA Update Channels - Ethernet

Update channel interface is a set of 10 differential signal pairs (five ports: includes both Receiver and Transmitter signals) that interconnect two slots. These signals are used to interconnect two hub boards, or redundant processor boards. The slots which need to be interconnected depend on the backplane design.

By default, the ATCA-7480 standard variant provides an EEPROM, which configures all four ports of the Intel i350 Ethernet controller for copper interface. Those are provided as 10/100/1000Base-T two 2x face plate RJ-45 and 2x ATCA Base-IFs on Zone 2.

If you need an Ethernet SERDES connection on ATCA Update channel, Port 0 requires a different Configuration EEPROM. For such Configuration EEPROM, you have to order it as a separate ATCA-7480 variant with a different order code. In this configuration, the Intel i350 Ethernet Port 2 is reconfigured from Copper Interface to SERDES interface. Therefore, the face plate Ethernet Port #1 will not be available with this EEPROM. This ATCA-7480 variant has a face plate with only 1x RJ-45 Ethernet port.

4.6 ATCA Fabric Interface Ethernet Controller

The ATCA-7480 blade utilizes two Intel XL710 Dual 40GB Ethernet controllers to provide four 40GB Ethernet IFs to the ATCA Zone 2. They operate at 40GBASE-KR4,10GBASE-KR,10GBASE-KX4,1000Base-KX: Option1, 1-K,1-KR, 9, 9-K, 9-KR. The redundant fabric I/F is fully operable in 40G, 10G, or 1G mode without the presence of an RTM.

Table 4-2 MAC Address Assignments

Board MAC Address#	Description	Ethernet Device	MAC Address Programmed at Device
N	i350 Port 0 (Base Channel 0)	U7	U62
N+1	i350 Port 1 (Base Channel 1)	U7	U62
N+2	i350 Port 2 (Front Panel RJ-45-1)	U7	U62
N+3	i350 Port 3 (Front Panel RJ-45-2)	U7	U62
N+4	XL710#1 Port 0 (Fabric Channel 0)	U4	U199
N+5	XL710#1 Port 1(Fabric Channel 2)	U4	U199
N+6	XL710#2 Port 0 (Fabric Channel 1)	U5	U202
N+7	XL710#2 Port 1 (Fabric Channel 3	U5	U202
N+8	IPMC MAC Address 1 (Base Channel 0)	U100	(FRU)
N+9	IPMC MAC Address 2 (Base Channel 1)	U100	(FRU)

4.7 Storage Controller

Using an optional RTM, the blade provides a Serial Attached SCSI (SAS) controller. One on-board hard disk drive (HDD) located on the RTM is connected to the controller. A minimum of two (2) ports are available on the RTM face plate. They can be used to attach an external storage RAID (JBOD). Another SAS port of the controller is routed to ATCA Zone 3 for synchronizing with an RTM-based disk located in a logically paired ATCA slot.

4.7.1 ATCA Update Channels - Storage

As described in section *ATCA Update Channels - Ethernet on page 93*, ATCA supports up to 10 differential signal pairs that can interconnect two hub boards or redundant processor boards. The ATCA-7480 uses one update channel for an Ethernet interconnect to another ATCA-7480 and for sharing storage interfaces between two redundant processor slots.

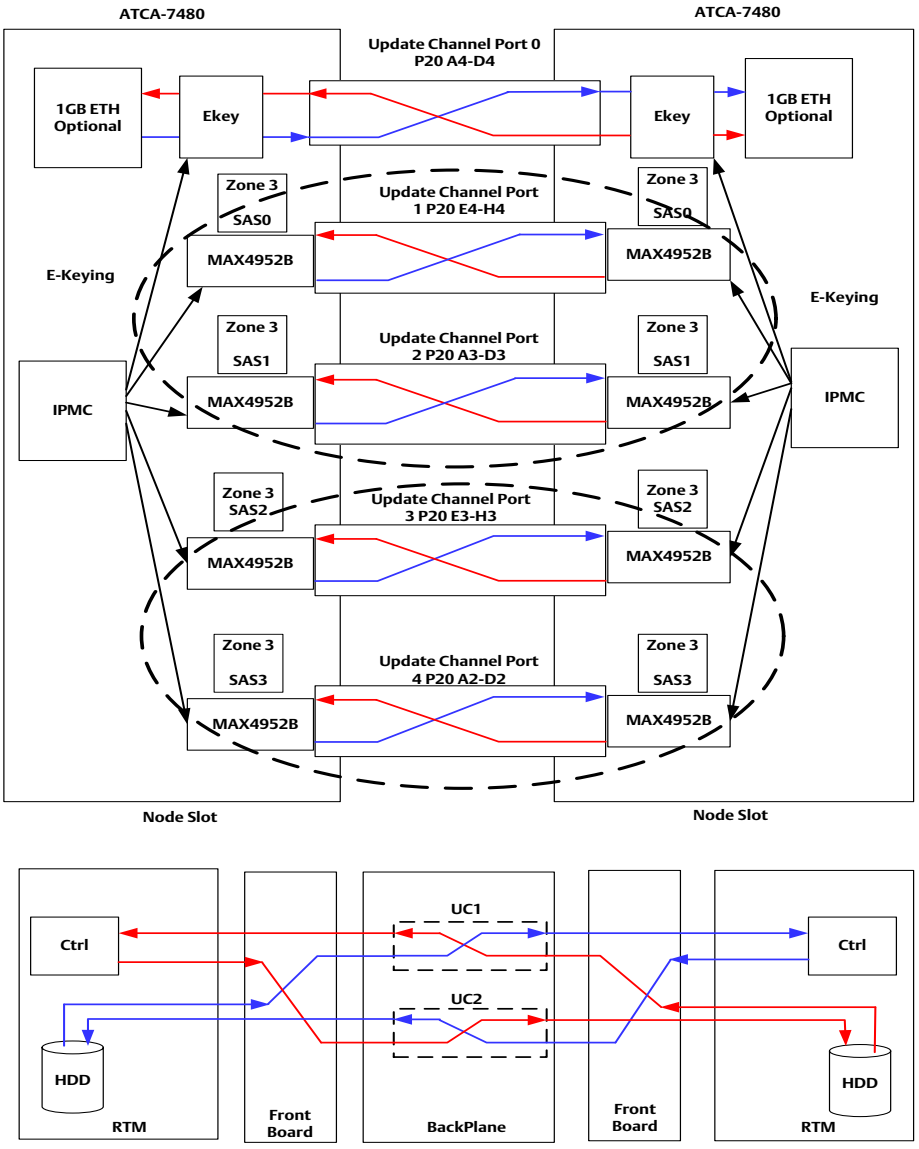
UC Port1-4 are connected to the Penguin Edge™ RTM series supporting SAS controller on RTM. Port1, 2 and Port 3, 4 connect an SAS controller port on RTM to a HDD on the RTM of the UC connected blade respectively.

NOTICE

By default, only SAS UC Port 1+2 is available. If you need SAS UC Port 3+4 and Ethernet UC Port 0, you have to order them separately.

The block diagrams in *Figure 4-2* illustrate the SAS update channel implementation. Basically, SAS controller and HDD reside on the RTM. There is a cross-connection link between a pair of SAS HDD and SAS Controller of two ATCA-7480 (with RTM) from Zone 3 to Zone 2 and connected through the backplane update channel to adjacent slot Zone 2 and back to Zone 3 of adjacent ATCA-7480 blade's RTM.

Figure 4-2 SAS Update Channel Implementation



4.8 MO297 SlimSATA Embedded Solid State Disc (SSD) Carrier/Riser Card

ATCA-7480 provides a modular solution for up to three MO297-A compliant SSDs. Each SSD is connected to the Intel Wellsburg PCH via a SATA interface. The modular approach consists of a riser card, which provide up to three sockets for SSDs and the MO297-A compliant SSDs. Before the storage solution can be mounted on ATCA-7480, the riser card and the SSDs have to be pre-mounted.

4.9 Heat Sink

Passive heat sinks are mounted on top of the Intel Haswell-EP LGA2011-R3 socket assembly. The maximum thermal design power used by Intel Haswell-EP is 75 W. The thermal resistance of the processor heat sink (including interface material) guarantees a proper cooling in the system. The heat sink fixture withstands shock and vibration tests.

4.10 BIOS

ATCA-7480 provides a BIOS firmware that is stored in flash memory. It can be updated remotely via Ethernet or locally via operating system. Along with the BIOS and BIOS Setup program, the flash memory contains POST and Plug and Play support.

The BIOS displays a message during POST identifying the type of BIOS and a revision code. A BIOS extension is provided for the RTM based SAS controller to support RAID configuration.

4.11 IPMC

ATCA-7480 contains the IPMC building block from Pigeon Point Systems (PPS). It is based on Microsemi Smartfusion cSOC (customizable System-on-Chip). The PPS IPMC controller is based on 32-bit Cortex M3 microcontroller operating at 50 MHz. The PPS implementation is the BMR-A2F200-AMCC-CM288R utilizing Microsemi Smartfusion A2F200M3F-CSG288I device.

4.11.1 I²C Bus

ATCA-7480 contains the IPMC controller Master-Only I²C Bus. It is also called as Private I²C Bus, which is connected to a FRU EEPROM, temperature sensors, and monitoring logic of the PIM.

Figure 4-3 Master Only I²C Bus Architecture

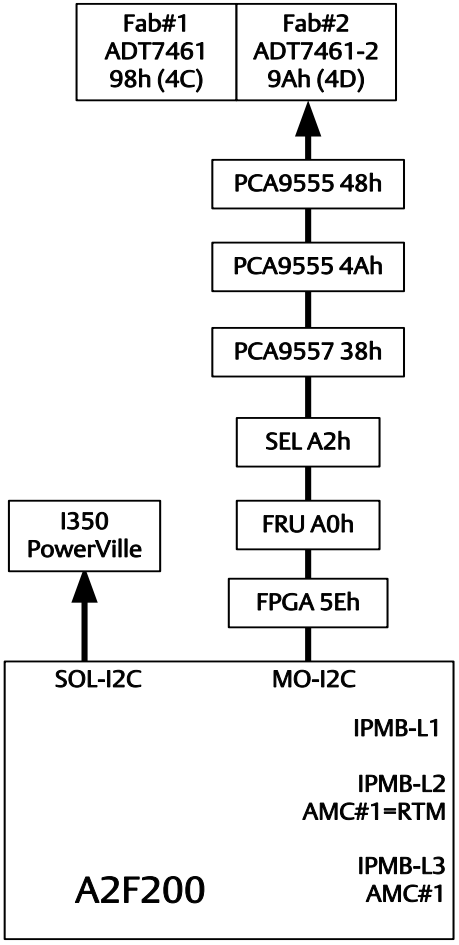


Table 4-3 IPMI I^2C Bus Address Map (Private I^2C Bus)

Device Name	Device Type	Location	I^2C Controller	SMB Address hex
IPMC Sensor #12 Inlet Temp	LM75	ATCA-7480	IPMB-L1	90
IPMC Sensor #13 Outlet Temp	LM75	ATCA-7480	IPMB-L1	94
48V Power Interface Sensor	PIM4328	ATCA-7480	IPMB-L1	50
FRU EEPROM	24C512	ATCA-7480	Atmel A2F200 Master-Only I^2C	A0
SEL EEPROM	24C512	ATCA-7480	Atmel A2F200 Master-Only I^2C	A2
GLUE FPGA	Lattice LFE2-6E	ATCA-7480	Atmel A2F200 Master-Only I^2C	FE
IPMC GPI I/O Expander#1	PCA9555	ATCA-7480	Atmel A2F200 Master-Only I^2C	48
IPMC GPI I/O Expander#2	PCA9555	ATCA-7480	Atmel A2F200 Master-Only I^2C	4A
IPMC GPI I/O Expander#1	PCA9557	ATCA-7480	Atmel A2F200 Master-Only I^2C	38
Intel XL710#1 Temp Sensor	ADT7461	ATCA-7480	Atmel A2F200 Master-Only I^2C	98
Intel XL710#1 Temp Sensor	ADT7461-2	ATCA-7480	Atmel A2F200 Master-Only I^2C	9A

4.11.2 FRU Data serial IDROM

ATCA-7480 contains a 64K Byte IDROM. It contains the FRU data, and board specific information. For example, serial number of the board, MAC addresses of network interfaces, and some additional information. The EEPROM has an I^2C interface and is connected to the on-board Private I^2C interface of IPMC building block. The IDROM is assigned to I^2C address 0xA0.

Characteristic	Value	I^2C Address
Device Type	24C512	$A0_H$

4.11.3 System Event Log EEPROM

ATCA-7480 contains a 64KByte System Event Log (SEL) PROM. The EEPROM has an I^2C interface and is connected to the on-board Private I^2C interface of IPMC building block. The IDROM is assigned to I^2C address 0xA2.

4.12 Serial Redirection

The CPU serial redirection reroutes the console input and output; that is the text output to the text screen and input from the standard keyboard. The console is used by the BIOS setup menus, BIOS initialization and boot routines, OS boot loaders, and the loaded OSs.

The serial console of the payload CPU is available via SOL. In addition to the SOL capability, the serial console is also available on the blade face plate using an RJ-45 connector with Cisco pin-out.

If an SOL session is established, only the output is available on the face plate. Input is not possible during this time via the face plate. Alternatively to the CPU serial console, the IPMC serial console is also available on the face plate serial connector. It can be selected via specific IPMI OEM command.

4.13 Serial Over LAN

Serial over LAN (SOL) enables suitably designed blades and servers to transparently redirect a serial character stream of a baseboard UART to/from a remote client via LAN over RMCP+ sessions. This enables users at remote consoles to access the serial port of a blade/server and interact with a text-based BIOS console, operating system, command line interfaces, and serial text-based applications.

The IPMC provides a dedicated sideband connection to the Base Interface Ethernet controller. This connectivity is not shared with IPMB-0 or any other I^2C/SMBus/IPMB connections that the IPMC may use on the blade for hardware management. Data from the payload serial redirection is routed through the sideband connection to the Base I/F and vice versa. The Ethernet controller filters packets based on either MAC address, RMCP port number, or IP address and forwards them to the serial redirection over the sideband interface.

Client software like openIPMI is required to enable SOL and to communicate with the SOL based serial console. Two additional MAC addresses are assigned to the board to support SOL connections on each of the base Interfaces. See the MAC address assignments in *Table 4-2 on page 93*.

4.14 Control Logic

The blade provides control logic for specific functions, which includes:

- Payload power supervision and sequencing
- Payload resets
- Multiple HW interfaces between payload and IPMC
- Support for sensors as required

Any control circuitry based on programmable logic whether intended for payload supervision or as part of the payload is remotely upgradeable. Crisis recovery circuitry is provided to prevent board lock-ups as the result of a failed remote upgrade of the board control logic.

4.15 Front Board Face Plate

The blade's face plate provides the following interfaces and control elements:

- Two USB 2.0 ports
- Two 10/1000/1000Base-T Ethernet ports
- Serial console port to connect to either payload or IPMC serial I/F
- Recessed reset button
- Out of Service, In Service, Attention, and Hot Swap LEDs

The blade design provides the possibility to cover unused face plate elements like LEDs or push button behind a custom overlay foil.

4.16 Face Plate Serial Interfaces

The ATCA-7480 has two serial interfaces. They are fully compliant to industry standard 16550 asynchronous communication controllers. The two Serial line interfaces #1 and #2 are integrated in the Intel DH8900CC PCH and routed to the on-board FPGA, which distributes them to either face plate, RTM, or IPMC for SOL. The serial line interfaces support baud rates up to 115200 kbps through a programmable baud rate generator.

Serial line interface #1 (COM #1) and #2 (COM#2) destination

The serial line interface #1/ #2 can be routed either to the Zone 3 connector or to the face plate. Destination selection is through IPMC or SW2-1.

The serial line interface #1 provides two different routing options:

- Glue Logic FPGA <=> RTM
- Glue Logic FPGA <=> Face plate

Table 4-4 Face Plate Serial Interfaces

SW2.1	Connection
HIGH Switch 2.1 OFF Default	Glue Logic FPGA COM1 to face plate Glue Logic FPGA COM2 to RTM
LOW or Switch 2.1 ON	Glue Logic FPGA COM1 to RTM Glue Logic FPGA COM2 to face plate

4.16.1 IPMC Debug Console

The IPMC Debug Console IF connection is normally routed to a 3-pin on-board header (RS232) The IPMC Debug monitor terminal output can also be routed to the face plate. The IPMC Debug Console is also available when the ATCA-7480 Payload is powered off.

Table 4-5 IPMC Debug Console Destination Selection

SW2.2	Connection
SW2.2 OFF Default	Face plate connected to Payload COM1/2 IPMC Debug Console at three Pin Header
SW2.2 ON	IPMC Debug Console to face plate

4.17 USB 3.0 Interfaces

The PCH Intel C612 (Wellsburg) provides internal USB 3.0/ USB 2.0 host controllers with up to six USB 3.0 ports (480Mb/s) and eight USB 2.0 ports. Two USB 2.0 ports are routed to the face plate and one USB 2.0 port is routed to the RTM. The ports available at the face plate are routed to a dual stacked connector. The ports are USB 3.0 compliant.

4.18 LPC Interface

The PCH provides a 4-bit-wide low pin count (LPC) interface running at 33MHz, which is connected to following on-board I/O devices:

- Glue Logic FPGA register map
- IPMC Controller
- TPM Extension Module Header

4.19 Trusted Platform Module

The Trusted Platform Module (TPM) is a specific protected and encapsulated microcontroller security chip used to defend the internal data structures against real intelligent attacks.

The nature of this security chip ensures that the information like keys, password, and digital certificates stored within are made more secure from external software attacks and physical theft. With the handful of keys it stores, all cryptographic functions are performed on the chip.

TPM provides the ability for a computing system to run applications more secured, allows secured remote access, performs electronic transactions and communication more safely.

The ATCA-7480 provides an on-board Infineon SLB9635TT1.2 FW3.16 TPM Controller connected to the LPC bus of PCH. This advanced Infineon controller guarantees that ATCA-7480 is fully compliant to TPM 1.2 specification. ATCA-7480 is ready to migrate to TPM 2.0.

4.20 Real Time Clock

An external 32.768kHz clock sources the internal real time clock inside Intel DH8900CC PCH with a frequency tolerance of 20 PPM. The RTC is fully DS1287, MC14618, PC87911, and Y2K compliant and provides 256 bytes of backed up CMOS RAM (of which 14 bytes contain the RTC time and date information and RTC configuration). During power down, the RTC consumes 0.µA/hr.

- Default power-down backup solution is an external +3V lithium battery with a capacity of 200mAh, which provides three years of backup.
- Optional power-down backup method uses a Super CAP with a 1 Farad capacity. This provides 300 hours of RTC/SRAM backup.

4.21 SMBus

Intel C612 PCH (Wellsburg) provides six SMBus interfaces. Only four interfaces are used on ATCA-7480 as described in the following table:

Table 4-6 SMBus Interface

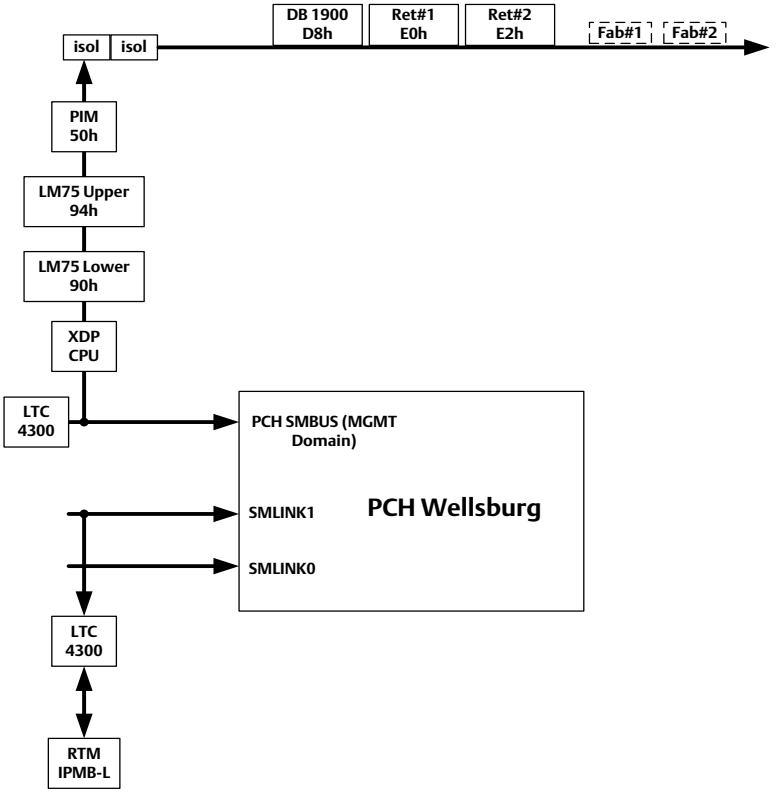
Device / SMBus	Description
Intel C612 B0:D31:F3	Host SMBus (Master/Slave)
SMLINK0	Connection to external IPMC to report thermal information via PCH internal PECI bridge to CPU
SMLink1	Reserved
ME SMBus	Optional connection

The Master SMBus interface of the Intel C612 PCH is connected to on-board devices like Clock PLLs, temperature sensors and so on. An I^2C Bus Repeater of type PCA9515 is used for load distribution and buffering.

Additionally, both CPUs provide 2x SMBus to connect to the SPD PROMs of the DDR4 memory system.

The following figure shows the ATCA-7480 SMBus architecture.

Figure 4-4 SMBus Architecture



The following table provides SMBus mapping address details.

Table 4-7 SMBus Address Map

Device Name	DeviceType	Location	SMBus Controller	SMB Address hex
SPD EEPROM	NA	DDR4 module	CPU#0 memory controller AB	A0
SPD EEPROM	NA	DDR4 module	CPU#0 memory controller AB	A8
SPD EEPROM	NA	DDR4 module	CPU#0 memory controller CD	A0

Table 4-7 SMBus Address Map (continued)

Device Name	DeviceType	Location	SMBus Controller	SMB Address hex
SPD EEPROM	NA	DDR4 module	CPU#0 memory controller CD	A8
SPD EEPROM	NA	DDR4 module	CPU#0 memory controller EF	A0
SPD EEPROM	NA	DDR4 module	CPU#0 memory controller EF	A8
SPD EEPROM	NA	DDR4 module	CPU#0 memory controller GH	A0
SPD EEPROM	NA	DDR4 module	CPU#0 memory controller GH	A8
IPMC Sensor #12 Inlet Temp	LM75	ATCA-7480	Intel Wellsburg PCH	90
IPMC Sensor #13 Outlet Temp	LM75	ATCA-7480	Intel Wellsburg PCH	94
48V Power Interface Sensor	PIM4328	ATCA-7480	Intel Wellsburg PCH	50
CB1900Z clock buffer	IDT 9ZX21901BKLF	ATCA-7480	Intel Wellsburg PCH	D8
Retimer #1	IDT 89HT0816	ATCA-7480	Intel Wellsburg PCH	E0
Retimer #2	IDT 89HT0816	ATCA-7480	Intel Wellsburg PCH	E2

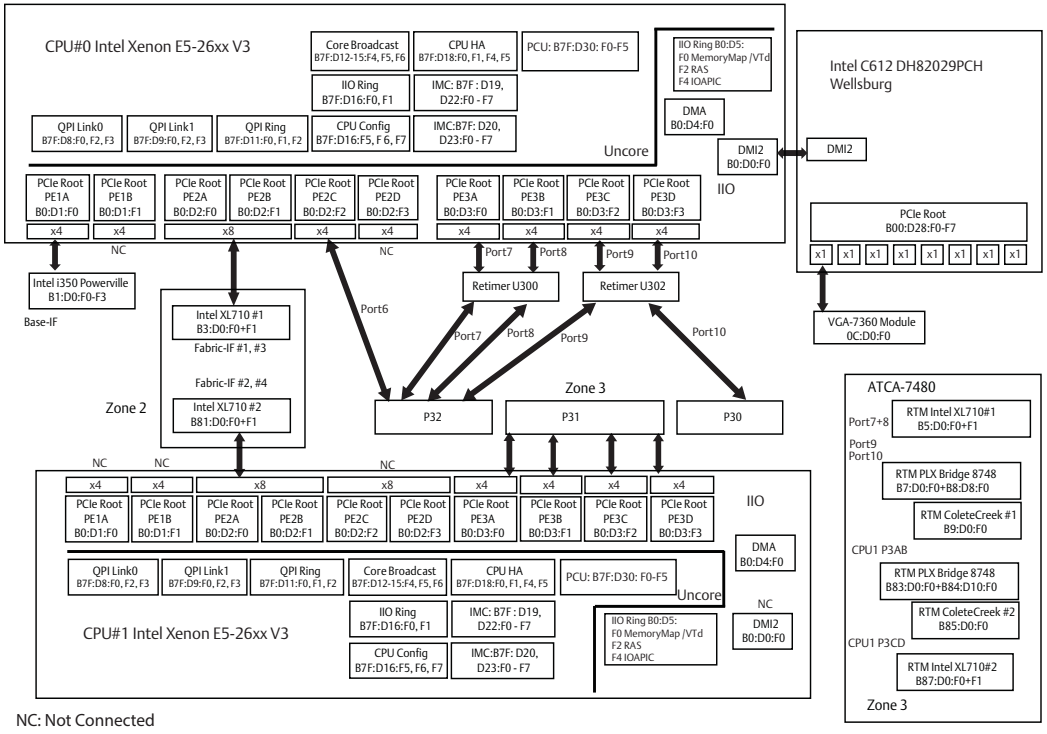
4.22 PCIe Bus Structure

The PCIe devices are connected through CPU0 (x40 PCIe), CPU1(x40 PCIe,) and PCH (x4 PCIe). In the figure, the notation is provided in **B**x:**D**y:**F**z format.

- B represents PCIe bus number (value of type Hexadecimal)
- D represents PCIe device (value of type Decimal)
- F represents Function

The following figure provides an overview of ATCA-7480 PCIe Bus structure.

Figure 4-5 PCIe Bus Structure



Maps and Registers

5.1 FPGA Registers

For register description, the conventions shown in *Table 5-1* and *Table 5-2* are used.

Table 5-1 Register Default

Default	Description
-	Not applicable or undefined
0 or 1	Default value after PWR_GOOD is valid or after PCH_PLTRST_ deassertion.
Undef.	Undefined value
<reset>: 0 or 1	Default value after deassertion of the reset signal <reset>
Ext.	External Reset Source. Default depends on external logic level.

Table 5-2 Register Access Type

Access	Description
r	Read only
w	Write only
r/w	Read and write
w1c	Write-1-to-clear, ignore bit while reading
r/w1c	Read and write-1-to-clear, write 0 has no effect
r/w1s	Read and write-1-to-set, write 0 has no effect
r/w1t	Read and write-1-to-toggle, write 0 has no effect
LPC:	The prefix “LPC:” signals that the access is restricted to the LPC interface. For example, LPC: r/w means that the register bit is readable/writable from the LPC interface
IPMC:	The prefix “IPMC:” signals that the access is restricted to the IPMC I^2C interface. For example, IPMC: r/w means that the register bit is readable/writable from IPMC I^2C interface

5.1.1 Register Decoding

The FPGA registers can be accessed from the host or the IPMC. For the host access, LPC bus interface is used. The IPMC uses an I^2C interface.

5.1.1.1 LPC Decoding

The LPC bus supports different protocols.

5.1.1.1.1 LPC I/O Decoding

The LPC interface responds to LPC I/O accesses listed in the following table. All other LPC I/O accesses are ignored.

Table 5-3 LPC I/O Register Map Overview

Base Address	Address Size	Address Range Name	Description
0x4E	2	SIW	Super IO Configuration Registers for Index and Date
0x80	1	POSTCODE	POST Code Register
BASE1	8	COM1	UART1. Serial Port 1 (Logical Device 4). BASE1 address is set up during Super IO Configuration.
BASE2	8	COM2	UART2. Serial Port 2. (Logical Device 4). BASE2 address is set up during Super IO Configuration.
0x600	128	REGISTERS	FPGA Registers

All LPC I/O accesses to address POSTCODE and the address range REGISTERS and within the address ranges of COM1 or COM2 (only when enabled during Super IO configuration) are decoded by the LPC core.

5.1.1.1.2 LPC Memory Decoding

The LPC interface never responds to LPC memory accesses.

5.1.1.1.3 LPC Firmware Decoding

The LPC interface never responds to LPC firmware accesses.

5.1.1.2 I²C Register Decoding

All I²C accesses from the IPMC towards the FPGA when the I²C master uses the I²C slave address 0x7F (the corresponding 8-bit slave address is 0xFE).

Table 5-4 IPMC SPI Register

I²C Address Range	Address Range Name	Description
0x00 - 0x7F	IPMC_REGISTERS	All FPGA registers which are accessible from IPMC

5.1.2 POST Code Register

The FPGA provides an 8 bit wide register to store POST codes to the LPC I/O address 0x80. The two nibbles of the register are converted to 7 segment codes and are displayed as two hex values by two 7 segment LED Displays.

The IPMC can read the POST code using the SPI interface (with the signal IPMC_SPI_SS_FPGA_ asserted) and the SPI address 0x7F.

The two 7 segment LED displays are also used for power failure indication.

Table 5-5 POST Code Register

LPC I/O Address: 0x80			
IPMC I²C Address: 0x7f			
Bit	**Description**	**Default**	**Access**
7:0	POST codes from host	0	LPC: r/w IPMC: r

5.1.3 Super IO Configuration Register

After an LPC Reset (PCH_PLTRST_ is asserted) or Power On Reset, the Super IO is in the Run Mode with the UARTs disabled. They may be configured using the LPC IO Address Range SIW (INDEX and DATA) by placing the Super IO into Configuration Mode. The BIOS uses these configuration addresses to initialize the logical devices at POST. The INDEX

and DATA addresses are only valid when the Super IO is in Configuration State. The INDEX and DATA addresses are effective only when the Super IO is in the Configuration State. When the Super IO is not in the Configuration State, reads return 0xFF and write data is ignored.

Table 5-6 Super IO Configuration Index Register

LPC I/O Address: 0x4E			
Bit	**Description**	**Default**	**Access**
7:0	INDEX. Configuration Index.	0xFF	LPC: r/w

Table 5-7 Super IO Configuration Data Register

LPC I/O Address: 0x4F			
Bit	**Description**	**Default**	**Access**
7:0	DATA Configuration Data.	0xFF	LPC: r/w

5.1.3.1 Entering the Configuration State

The device enters the Configuration State by the following contiguous sequence:

1. Write 80H to Configuration Index Port.
2. Write 86H to Configuration Index Port.

5.1.3.2 Existing the Configuration State

The device exits the Configuration State by the following contiguous sequence:

1. Write 68H to Configuration Index Port.
2. Write 08H to Configuration Index Port.

5.1.3.3 Configuration Mode

The system sets the logical device information and activates desired logical devices through the INDEX and DATA ports.

The desired configuration registers are accessed in two steps:

1. Write the index of the Logical Device Number Configuration Register (i.e., 07) to the INDEX PORT and then write the number of the desired logical device to the DATA PORT.

2. Write the address of the desired configuration register within the logical device to the INDEX PORT and then write or read the configuration register through the DATA PORT.

NOTICE

If accessing the Global Configuration Registers, step (1) is not required. The Super IO returns to the RUN state.

Only two states are defined (Run and Configuration). In the Run State the Super IO is always ready to enter the Configuration state.

5.1.3.4 Super IO Configuration Registers

Address locations that are not listed are considered reserved register locations. Reads to reserved registers may return non-zero values. Writes to reserved locations may cause system failure.

5.1.3.4.1 Global Control Configuration Registers

The Super IO Global Registers lie in the address range 0x00-0x2F. All eight bits of the ADDRESS Port are used for register selection. All unimplemented registers and bits ignore writes and return zero when read. The INDEX PORT is used to select a configuration register in the chip. The DATA PORT is then used to access the selected register. These registers are accessible only in the Configuration Mode.

Table 5-8 Global Configuration Register Summary

Index Address	Description
0x07	Super IO Logical Device Number
0x20	Super IO Device ID
0x21	Super IO Device Revision
0x28	Super IO LPC Control
0x29	Super IO SERIRQ and Pre-divide Control

Table 5-9 Super IO Logical Device Number Register

Index Address: 0x07			
Bit	**Description**	**Default**	**Access**
7:0	Logical Device Number: 0x04: Logical Device 4 (UART 1Serial Port 1) 0x05: Logical Device 5 (UART2 Serial Port 2) A write to this register selects the current logical device. This allows access to the control and configuration registers for each logical device.	0	LPC: r/w

Table 5-10 Super IO Device Identification Register

Index Address: 0x20			
Bit	**Description**	**Default**	**Access**
7:0	Device ID	0x0	LPC: r

Table 5-11 Super IO Device Revision Register

Index Address: 0x21			
Bit	**Description**	**Default**	**Access**
7:0	Device Revision	0x01	LPC: r

Table 5-12 Super IO LPC Control Register

Index Address: 0x28			
Bit	**Description**	**Default**	**Access**
0	LPC Bus Wait States: 1: Long wait states (sync 6)	1	LPC: r
7:1	Reserved	0	LPC: r

Table 5-13 Global Super IO SERIRQ and Pre-divide Control Register

Index Address: 0x29			
Bit	**Description**	**Default**	**Access**
0	SERIRQ enable: 0: disabled. Serial interrupts disabled. 1: enabled. Logical devices participate in interrupt generations.	0	LPC: r/w
1	SERIRQ Mode: 1: Continuous Mode	1	LPC: r
3:2	UART Clock pre-divide 00: divide by 1 01: divide by 8 10: divide by 26 (CLK_UART is 48 MHz) 11: reserved	0	LPC: r/w
7:4	Reserved	0	LPC: r

5.1.3.4.2 Logical Device Configuration Registers

Use to access the registers that are assigned to each logical unit. The Super IO supports two logical units and has two sets of logical device registers. The two logical devices are UART1 (Logical Number 4) and UART2 (Logical Number 5). A separate set (bank) of control and configuration registers exists for each logical device and is selected with the Logical Device Number Register. The INDEX PORT is used to select a specific logical device register. These registers are then accessed through the DATA PORT. The Logical Device registers are accessible only when the device is in the Configuration state.

Table 5-14 Logical Device Configuration Register Summary

Index Address	Description
0x30	Enable
0x60	Base IO Address MSB
0x61	Base IO Address LSB
0x70	Primary Interrupt Select
0x74	Reserved
0x75	Reserved
0xF0	Reserved

The logical register addresses are shown in the tables below:

Table 5-15 Logical Device Enable Register

Index Address: 0x30			
Bit	**Description**	**Default**	**Access**
0	Logical Device Enable: 0: disabled. Currently selected device is inactive. 1: enabled. The currently selected device is enabled.	1	LPC: r/w
7:1	Reserved	0	LPC: r

Table 5-16 Logical Device Base IO Address MSB Register

Index Address: 0x60			
Bit	**Description**	**Default**	**Access**
7:0	Logical Device Base IO Address MSB	0	LPC: r/w

Table 5-17 Logical Device Base IO Address LSB Register

Index Address: 0x61			
Bit	**Description**	**Default**	**Access**
2:0	Bits 0 to 2 are read only. Decode is on 8 Byte boundary.	0	LPC: r
7:3	Logical Device Base IO Address LSB. (Bits 3 to 7)	0	LPC: r/w

Registers 0x60 (MSB) and 0x61 (LSB) set the Logical Device Base IO for this logical device. For example, for Base IO address 0x3F8 the content of Register 0x60 is 0x03 and the content of Register 0x61is 0xF8.

See *Table 5-18* below for Common Decode Ranges:

Table 5-18 Logical Device Common Decode Ranges

IO Address Range	Description
0x3F8 - 0x3FF	COM1
0x2F8 - 0x2FF	COM2
0x2E8 - 0x2EF	COM3
0x3E8 - 0x3EF	COM4

Table 5-19 Logical Device Primary Interrupt Register

Index Address: 0x70			
Bit	**Description**	**Default**	**Access**
3:0	Interrupt level is used for Primary Interrupt 0x0: no interrupt selected 0x1: IRQ1 0x2: IRQ2 0x3: IRQ3 0x4: IRQ4 0x5: IRQ5 0x6: IRQ6 0x7: IRQ7 0x8: IRQ8 0x9: IRQ9 0xA: IRQ10 0xB: IRQ11 0xC: IRQ12 0xD: IRQ13 0xE: IRQ14 0xF: IRQ15	0	LPC: r/w
7:4	Reserved	0	LPC: r

NOTICE

An Interrupt is activated by enabling this device (offset 0x30), setting this register to a non-zero value and setting any combination of bits 0-4 in the corresponding UART IER and the occurrence of the corresponding UART event (i.e., Modem Status Change, Receiver Line Error Condition, Transmit Data Request, Receiver Data Available or Receiver Time Out) and setting the OUT2 bit in the MCR.

Table 5-20 Logical Device 0x74 Reserved Register

Index Address: 0x74			
Bit	**Description**	**Default**	**Access**
7:0	Reserved	0x04	LPC: r

Table 5-21 Logical Device 0x75 Reserved Register

Index Address: 0x75			
Bit	**Description**	**Default**	**Access**
7:0	Reserved	0x04	LPC: r

Table 5-22 Logical Device 0xF0 Reserved Register

Index Address: 0xF0			
Bit	**Description**	**Default**	**Access**
7:0	Reserved	0	LPC: r

5.1.4 UART1 and UART2 Register Map

The LPC IO Base addresses BASE1 for UART1 and BASE2 for UART2 are set up during Super IO configuration. See *Super IO Configuration Register on page 109*.

5.1.4.1 UART Register Overview

Table 5-23 shows the registers and their addresses as offsets of a base address for one of the two UARTs.

The state of the Divisor Latch Bit (DLAB), which is the MOST significant bit of the Serial Line Control Register (SCR), affects the selection of certain of the UART registers. The DLAB bit must be set high by the system software to access the Baud Rate Generator Divisor Latches (DLL and DLM).

Table 5-23 UART Register Overview

LPC IO Address	DLAB Bit value	Description
Base	0	Receiver Buffer (RBR). Read Only
Base	0	Transmitter Holding (THR). Write Only.
Base + 1	0	Interrupt Enable Register (IER)
Base + 2	X	Interrupt Identification Register (IIR). Read Only
Base + 2	X	FIFO Control Register (FCR). Write Only.
Base + 3	X	Line Control Register (LCR)

Table 5-23 UART Register Overview (continued)

LPC IO Address	DLAB Bit value	Description
Base + 4	X	Modem Control Register (MCR)
Base + 5	X	Line Status Register (LSR). Read Only
Base + 6	X	Modem Status Register (MSR). Read Only
Base + 7	X	Scratch Pad Register (SCR).
Base	1	Divisor Latch LSB (DLL)
Base + 1	1	Divisor Latch MSB (DLM)

5.1.4.2 UART Registers DLAB=0

5.1.4.2.1 Receiver Buffer Register (RBR)

In non-FIFO mode, this register holds the character received by the UART's Receive Shift Register. If fewer than eight bits are received, the bits are right-justified and the leading bits are zeroed. Reading the register, empties the register and resets the Data Ready (DR) bit in the Line Status Register to zero. Other (error) bits in the Line Status Register are not cleared. In FIFO mode, this register latches the value of the data byte at the top of the FIFO.

Table 5-24 Receiver Buffer Register (RBR) if DLAB=0

LPC IO Address: Base			
Bit	**Description**	**Default**	**Access**
7:0	Receiver Buffer register (RBR)	Undef.	LPC: r

5.1.4.2.2 Transmitter Holding Register (THR)

This register holds the next data byte to be transmitted. When the Transmit Shift Register becomes empty, the contents of the Transmit Holding Register are loaded into the shift register and the transmit data request (TDRQ) bit in the Line Status Register is set to one.

Table 5-25 Transmitter Holding Register (THR) if DLAB=0

LPC IO Address: Base			
Bit	**Description**	**Default**	**Access**
7:0	Transmitter Holding register (THR)	Undef.	LPC: w

In FIFO mode, writing to THR puts data to the top of the FIFO. The data at the bottom of the FIFO is loaded to the shift register when it is empty.

5.1.4.2.3 Interrupt Enable Register (IER)

This register enables four types of interrupts which independently activate the int signal and set a value in the Interrupt Identification Register. Each of the four interrupt types can be disabled by resetting the appropriate bit of the IER register. Similarly, by setting the appropriate bits, selected interrupts can be enabled.

Table 5-26 Interrupt Enable Register (IER), if DLAB=0

LPC IO Address: Base + 1			
Bit	**Description**	**Default**	**Access**
0	Receive data interrupt enable/disable: 1: receive data interrupt enabled 0: receive data interrupt disabled	0	LPC: r/w
1	Transmitter holding register empty (THRE) interrupt enable/disable 1: THRE interrupt enabled 0: THRE interrupt disabled	0	LPC: r/w
2	Receiver line status interrupt enable/disable 1: receiver line status interrupt enabled 0: receiver line status interrupt disabled	0	LPC: r/w
3	Modem status interrupt enable/disable: 1: modem status interrupt enabled 0: modem status interrupt disabled	0	LPC: r/w
7:4	Reserved	0	LPC: r

5.1.4.2.4 Interrupt Identification Register (IIR)

In order to minimize software overhead during data character transfers, the UART prioritizes interrupts into four levels (listed in the following table) and records these in the Interrupt Identification Register. The Interrupt Identification Register (IIR) stores information indicating that a prioritized interrupt is pending and the source of that interrupt.

Table 5-27 UART Interrupt Priorities2

Priority Level	Interrupt Source
1 (highest)	Receiver Line Status. One or more error bits were set.
2	Received Data is available. In FIFO mode, trigger level was reached; in non-FIFO mode, RBR has data.
2	Receiver Time out occurred. It happens in FIFO mode only, when there is data in the receive FIFO but no activity for a time period.
3	Transmitter requests data. In FIFO mode, the transmit FIFO is half or more than half empty; in non-FIFO mode, THR is read already
4	Modem Status: one or more of the modem input signals has changed state

Table 5-28 Interrupt Identification Register (IIR)

LPC IO Address: Base + 2			
Bit	**Description**	**Default**	**Access**
0	Interrupt status bit: 1: no interrupt pending 0: interrupt pending	1	LPC: r
2:1	Interrupt priority level and source: 11: Receiver line status 10: Receiver data available 01: Transmitter holding register empty 00: Modem status	0	LPC: r
3	Time Out Detected: 0: No time out interrupt is pending 1: Character time-out indication (FIFO mode only)	0	LPC: r
5:4	Reserved	0	LPC: r
7:6	FIFO Mode Enable bits: 00: Default mode 01: Reserved 10: Reserved 11: FIFO mode	0	LPC: r

Table 5-29 Interrupt Identification Register Decode

Interrupt ID	Interrupt Set/Reset Function			
3:0	**Priority**	**Type**	**Source**	**Reset Control**
0b0001	-	None	No Interrupt is pending	-
0b0110	1	Receiver Line Status	Overrun Error, Parity Error, Framing Error, Break Interrupt.	Reading the Line Status Register.
0b0100	2	Received Data Available	Non-FIFO mode: Receive Buffer is full.	Non-FIFO mode: Reading the Receiver Buffer Register.
			FIFO mode: Trigger level was reached.	FIFO mode: Reading bytes until Receiver FIFO drops below trigger level or setting RESETRF bit in FCR register.
0b1100		Character Timeout indication	FIFO Mode only: At least 1 character is in receiver FIFO and there was no activity for a time period.	Reading the Receiver FIFO or setting RESETRF bit in FCR register
0b0010	3	Transmit FIFO Data Request	Non-FIFO mode: Transmit Holding Register Empty	Reading the IIR Register (if the source of the interrupt) or writing into the Transmit Holding Register.
			FIFO mode: Transmit FIFO has half or less than half data.	Reading the IIR Register (if the source of the interrupt) or writing to the Transmitter FIFO.
0b0000	4	Modem Status	Clear to Send, Data Set Ready, Ring Indicator, Received Line Signal Detect	Reading the modem status register

5.1.4.2.5 FIFO Control Register (FCR)

FCR is a write-only register that is located at the same address as the IIR (IIR is a read-only register). FCR enables/disables the transmitter/receiver FIFOs, clears the transmitter/receiver FIFOs, and sets the receiver FIFO trigger level.

Table 5-30 FIFO Control Register (FCR)

LPC IO Address: Base + 2			
Bit	**Description**	**Default**	**Access**
0	FIFO enable/disable: 1: Transmitter and Receiver FIFO enabled 0: FIFO disabled	0	LPC: w
1	Receiver FIFO reset: 1: Bytes in receiver FIFO and counter are reset. Shift register is not reset (bit is self-clearing) 0: No effect	0	LPC: w
2	Transmit FIFO reset: 1: Bytes in receiver FIFO and counter are reset. Shift register is not reset (bit is self-clearing) 0: No effect	0	LPC: w
3	Receiver/Transmitter ready. Not supported.	0	LPC: w
5:4	Reserved	0	LPC: w
7:6	Receiver FIFO interrupt trigger level: 00: 1 byte 01: 4 bytes 10: 8 bytes 11: 14 bytes	0	LPC: w

5.1.4.2.6 Line Control Register (LCR)

In the Line Control Register (LCR), the system programmer specifies the format of the asynchronous data communications exchange. The serial data format consists of a start bit (logic 0), five to eight data bits, an optional parity bit, and one or two stop bits (logic 1). The LCR has bits for accessing the Divisor Latch and causing a break condition. The programmer can also read the contents of the Line Control Register. The read capability simplifies system programming and eliminates the need for separate storage in system memory.

Table 5-31 Line Control Register (LCR)

LPC IO Address: Base + 3			
Bit	**Description**	**Default**	**Access**
1:0	Serial character WORD length: 00: 5 bits 01: 6 bits 10: 7 bits 11: 8 bits	0	LPC: r/w
2	Stop bit length: 1: 1.5 stop bits for 5 bit WORD length 1: 2 stop bits for 6, 7, and 8 bit WORD length 0: 1 stop bit for any serial character WORD length	0	LPC: r/w
3	Parity enable/disable When bit 3 is set, a parity bit is generated in transmitted data between the last data WORD bit and the first stop bit. In received data, if bit 3 is set, parity is checked. When bit 3 is cleared, no parity is generated or checked.: 1: Parity enabled 0: Parity disabled	0	LPC: r/w
4	Parity even/odd When parity is enabled and bit 4 is set, even parity (an even number of logic ones in the data and parity bits) is selected. When parity is disabled and bit 4 is cleared, odd parity (an odd number of logic ones) is selected.: 1: Even parity 0: Odd parity	0	LPC: r/w

Table 5-31 Line Control Register (LCR) (continued)

LPC IO Address: Base + 3			
Bit	**Description**	**Default**	**Access**
5	Stick parity When bits 3, 4, and 5 are set, the parity bit is transmitted and checked as cleared. When bits 3 and 5 are set and bit 4 is cleared, the parity bit is transmitted and checked as set. If bit 5 is cleared, stick parity is disabled.: 1: Stick parity enabled 0: Stick parity disabled	0	LPC: r/w
6	Break control bit Bit 6 is set to force a break condition, i.e. a condition where TXD is forced to the spacing (cleared) state. When bit 6 is cleared, the break condition is disabled and has no affect on the transmitter logic. It only effects TXD: 1: Break condition enabled 0: Break condition disabled	0	LPC: r/w
7	Divisor latch access bit (DLAB) Bit 7 must be set to access the divisor latches of the baud generator during a read or write. Bit 7 must be cleared during a read or write to access the RBR, THR, or IER.: 1: Access to DLL and DLM registers 0: Access to RBR, THR and IER registers	0	LPC: r/w

5.1.4.2.7 Modem Control Register (MCR)

This 8-bit register controls the interface with the modem or data set (or a peripheral device emulating a modem).

Table 5-32 Modem Control Register (MCR)

LPC IO Address: Base + 4			
Bit	**Description**	**Default**	**Access**
0	Data terminal ready (DTR#) output control: 1: DTR# output in low (active) state 0: DTR# output in high state	0	LPC: r/w

Table 5-32 Modem Control Register (MCR) (continued)

LPC IO Address: Base + 4			
Bit	**Description**	**Default**	**Access**
1	Request to send (#) output control: 1: # output in low (active) state 0: # output in high state	0	LPC: r/w
2	User output control signal (OUT1#): 1: OUT1# output in high state 0: OUT1# output in low state Not supported	0	LPC: r/w
3	User output control signal (OUT2#): 1: OUT2# output in high state 0: OUT2# output in low state Not supported	0	LPC: r/w
4	Local loop back diagnostic control When loop back is activated: Transmitter TXD is set high. Receiver RXD is disconnected. Output of Transmitter Shift register is looped back into the receiver shift register input. Modem control inputs are disconnected Modem control outputs are internally connected to modem control inputs. Modem control outputs are forced to the inactive (high) levels: 1: Loop back mode activated 0: Normal operation	0	LPC: r/w
5	Autoflow control enable (AFE): 1: Autoflow control enabled (auto-# and auto-CTS# or auto-CTS# only enabled) 0: Autoflow control disabled	0	LPC: r/w
7:6	Reserved	0	LPC: r

5.1.4.2.8 Line Status Register (LSR)

This register provides status information to the processor concerning the data transfers. Bits 5 and 6 show information about the transmitter section. The rest of the bits contain information about the receiver.

In non-FIFO mode, three of the LSR register bits, parity error, framing error, and break interrupt, show the error status of the character that has just been received. In FIFO mode, these three bits of status are stored with each received character in the FIFO. LSR shows the status bits of the character at the top of the FIFO. When the character at the top of the FIFO has errors, the LSR error bits are set and are not cleared until software reads LSR, even if the character in the FIFO is read and a new character is now at the top of the FIFO.

Bits one through four are the error conditions that produce a receiver line status interrupt when any of the corresponding conditions are detected and the interrupt is enabled. These bits are not cleared by reading the erroneous byte from the FIFO or receive buffer. They are cleared only by reading LSR. In FIFO mode, the line status interrupt occurs only when the erroneous byte is at the top of the FIFO. If the erroneous byte being received is not at the top of the FIFO, an interrupt is generated only after the previous bytes are read and the erroneous byte is moved to the top of the FIFO.

Table 5-33 Line Status Register (LSR)

LPC IO Address: Base + 5			
Bit	**Description**	**Default**	**Access**
0	Receiver data ready (DR) indicator DR is set whenever a complete incoming character has been received and transferred into the RBR or the FIFO. DR is cleared by reading all of the data in the RBR or the FIFO: 1: New data received 0: No new data	0	LPC: r
1	Overrun error (OE) indicator When OE is set, it indicates that before the character in the RBR was read, it was overwritten by the next character transferred into the register. OE is cleared every time the CPU reads the contents of the LSR. If the FIFO mode data continues to fill the FIFO beyond the trigger level, an overrun error occurs only after the FIFO is full and the next character has been completely received in the shift register. An overrun error is indicated to the CPU as soon as it happens. The character in the shift register is overwritten but it is not transferred to the FIFO: 1: Overrun error occurred 0: No overrun error	0	LPC: r

Table 5-33 Line Status Register (LSR) (continued)

LPC IO Address: Base + 5			
Bit	**Description**	**Default**	**Access**
2	Parity Error (PE) indicator When PE is set, it indicates that the parity of the received data character does not match the parity selected in the LCR (bit 4). PE is cleared every time the CPU reads the contents of the LSR. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO: 1: Parity error occurred 0: No parity error	0	LPC: r
3	Framing Error (FE) indicator When FE is set, it indicates that the received character did not have a valid (set) stop bit. FE is cleared every time the CPU reads the contents of the LSR. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO. The ACE tries to resynchronize after a framing error. To accomplish this, it is assumed that the framing error is due to the next start bit. The ACE samples this start bit twice and then accepts the input data: 1: Framing error occurred 0: No framing error	0	LPC: r
4	Break Interrupt (BI) indicator When BI is set, it indicates that the received data input was held low for longer than a full-word transmission time. A full-word transmission time is defined as the total time to transmit the start, data, parity, and stop bits. BI is cleared every time the CPU reads the contents of the LSR. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO. When a break occurs, only one 0 character is loaded into the FIFO. The next character transfer is enabled after RXD goes to the marking state for at least two Receiver CLK samples and then receives the next valid start bit: 1: Full WORD transmission time exceeded 0: Normal operation	0	LPC: r

Table 5-33 Line Status Register (LSR) (continued)

LPC IO Address: Base + 5			
Bit	**Description**	**Default**	**Access**
5	Transmit Holding Register Empty (THRE) indicator THRE is set when the THR is empty, indicating that the ACE is ready to accept a new character. If the THRE interrupt is enabled when THRE is set, an interrupt is generated. THRE is set when the contents of the THR are transferred to the TSR. THRE is cleared concurrent with the loading of the THR by the CPU. In the FIFO mode, THRE is set when the transmit FIFO is empty; it is cleared when at least one byte is written to the transmit FIFO: 1: THR/Transmit FIFO empty 0: THR/Transmit FIFO contains data	1	LPC: r
6	Transmitter Empty (TEMT) indicator TEMT bit is set when the THR and the TSR are both empty. When either the THR or the TSR contains a data character, TEMT is cleared. In the FIFO mode, TEMT is set when the transmitter FIFO and shift register are both empty: 1: THR/Transmit FIFO/TSR empty 0: THR/Transmit FIFO/TSR contains data	1	LPC: r
7	FIFO data error In the FIFO mode, LSR7 is set when there is at least one parity, framing, or break error in the FIFO. It is cleared when the microprocessor reads the LSR and there are no subsequent errors in the FIFO. If FIFO is not used, bit always reads 0: 1: FIFO data error encountered 0: No FIFO error encountered	0	LPC: r

5.1.4.2.9 Modem Status Register (MSR)

This 8-bit register provides the current state of the control lines from the modem or data set (or a peripheral device emulating a modem) to the processor. In addition to this current state information, four bits of the Modem Status Register provide change information. Bits 03:00 are set to a logic 1 when a control input from the Modem changes state. They are reset to a logic 0 when the processor reads the Modem Status Register.

When bits 0, 1, 2, or 3 are set to logic 1, a Modem Status interrupt is generated if bit 3 of the Interrupt Enable Register is set.

Table 5-34 Modem Status Register (MSR)

LPC IO Address: Base + 6			
Bit	**Description**	**Default**	**Access**
0	Change in clear-to-send (DCTS) indicator DCTS indicates that the CTS# input has changed state since the last time it was read by the CPU. When DCTS is set (autoflow control is not enabled and the modem status interrupt is enabled), a modem status interrupt is generated. When autoflow control is enabled (DCTS is cleared), no interrupt is generated: 1: Change in state of CTS# input since last read 0: No change in state of CTS# input since last read	0	LPC: r/w
1	Change in data set ready (DDSR) indicator DDSR indicates that the DSR# input has changed state since the last time it was read by the CPU. When DDSR is set and the modem status interrupt is enabled, a modem status interrupt is generated: 1: Change in state of DSR# input since last read 0: No change in state of DSR# input since last read	0	LPC: r/w
2	Trailing edge of the ring indicator (TERI) detector TERI indicates that the RI# input to the chip has changed from a low to a high level. When TERI is set and the modem status interrupt is enabled, a modem status interrupt is generated. Not supported.	0	LPC: r/w
3	Change in data carrier detect (DDCD) indicator DDCD indicates that the DCD# input to the chip has changed state since the last time it was read by the CPU. When DDCD is set and the modem status interrupt is enabled, a modem status interrupt is generated. Not supported.	0	LPC: r/w

Table 5-34 Modem Status Register (MSR) (continued)

LPC IO Address: Base + 6			
Bit	**Description**	**Default**	**Access**
4	Complement of the clear-to-send (CTS#) input When the Asynchronous Communications Element (ACE) is in diagnostic test mode (LOOP [MCR4] = 1), this bit is equal to the MCR bit 1 (#).	Ext.	LPC: r
5	Complement of the data set ready (DSR#) input When the ACE is in the diagnostic test mode (LOOP [MCR4] = 1), this bit is equal to the MCR bit 0 (DTR#).	Ext.	LPC: r
6	Complement of the ring indicator (RI#) input When the ACE is in the diagnostic test mode (LOOP [MCR4] = 1), this bit is equal to the MCR bit 2 (OUT1#). Not supported.	Ext.	LPC: r
7	Complement of the data carrier detect (DCD#) input When the ACE is in the diagnostic test mode (LOOP [MCR4] = 1), this bit is equal to the MCR bit 3 (OUT2#). Not supported.	Ext.	LPC: r

5.1.4.2.10 Scratch Register (SCR)

This 8-bit read/write register has no effect on the UART. It is intended as a scratch pad register for use by the programmer.

Table 5-35 Scratch Register (SCR)

LPC IO Address: Base + 7			
Bit	**Description**	**Default**	**Access**
7:0	Scratch Register (SCR) The scratch register is an 8 bit register that is intended for the programmer's use as a scratch pad in the sense that it temporarily holds the programmer's data without affecting any other ACE operation.	Undef.	LPC: r/w

5.1.4.3 Programmable Baud Rate Generator

The UART contains a programmable Baud Rate Generator that is capable of taking the UART_CLK input and dividing it by any divisor from 1 to (2^{16}-1). The output frequency of the Baud Rate Generator is 16 times the baud rate. Two 8-bit latches store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization to ensure proper

operation of the Baud Rate Generator. If both divisor latches are loaded with 0, the 16X output clock is stopped. Upon loading either of the divisor latches, a 16-bit baud counter is immediately loaded. This prevents long counts on initial load. Access to the divisor latch can be done with a word write.

The UART_CLK is the CLK_UART (48MHz) input divided by the pre-divider set by the Super IO Configuration Register (Offset 0x29).

The baud rate of the data shifted in/out of the UART is given by:

Baud Rate = UART_CLK */ (16X Divisor)*

For example, if the pre-divider is 26, the UART_CLK is 1.8461538MHz. When the divisor is 12, the baud rate is 9600.

A divisor value of 0 in the Divisor Latch Register is not allowed.

Table 5-36 Divisor Latch LSB Register (DLL), if DLAB=1

PC IO Address: Base			
Bit	**Description**	**Default**	**Access**
7:0	Divisor Latch LSB (DLL)	Undef.	LPC: r/w

Table 5-37 Divisor Latch MSB Register (DLM), if DLAB=1

LPC IO Address: Base + 1			
Bit	**Description**	**Default**	**Access**
7:0	Divisor Latch MSB (DLM)	Undef.	LPC: r/w

5.1.5 FPGA Register Mapping

5.1.5.1 LPC I/O Register Map

The FPGA registers can be accessed via LPC I/O cycles in the I/O address range REGISTERS. See *Table 5-38* FPGA Register Map Overview. For a LPC register access the host uses the base address, 0x600. Individual registers can be accessed by adding an offset to the base address. An LPC I/O write access to an address not listed in this table or marked with an "-" in the LPC I/O column is ignored. A corresponding read access delivers always zero – used and reserved for future extensions. A reserved register is read only and deliver always zero. A reserved bit is read-only and always reads zero.

NOTICE
LPC I/O Address = 0x600 + Address Offset

5.1.5.2 IPMC I^2C Register Map

Some FPGA registers may be accessed via IPMC Private I^2C transactions (Slave address 0x7F). See *Table 5-38* FPGA Register Map Overview. An IPMC write access to an address not listed in this table or marked with an "-" in the IPMC I^2C column is ignored. A corresponding read access delivers always zero. The address offsets not mentioned below are not used and reserved for future extensions. A reserved register is read-only and always deliver zero. A reserved bit is read-only and always reads zero.

Table 5-38 FPGA Register Map Overview

LPC Address Offset	LPC I/O	IPMC I^2C	Description
0x00-0x01	r	r	Module Identification Register (*Table 5-39*)
0x02	r	r	FPGA Version Register (*Table 5-40*)
0x03	r/w	r	Serial Redirection Control Register (*Table 5-41*)
0x04	r	r/w	Serial over LAN Control Register (*Table 5-42*)
0x05	r	r/w	Serial Line Routing Register (*Table 5-43*)
0x06	r	r/w	IPMC Power Level Register
0x07	r	r/w	IPMC Power Level Multiplier Register
0x08	-	r	ME Power Failure State Register (*Table 5-44*)

Table 5-38 FPGA Register Map Overview (continued)

LPC Address Offset	LPC I/O	IPMC I^2C	Description
0x09	-	r	ME Power Failure Cause Register (*Table 5-46*)
0x0A	-	r	Payload Power Failure State Register (*Table 5-47*)
0x0B	-	r	Payload Power Failure Cause Register 1 (*Table 5-49*)
0x0C	-	r	Payload Power Failure Cause Register 2 (*Table 5-50*)
0x0D	-	r	Payload Power Failure Cause Register 3 (*Table 5-51*)
0x0E	-	r	Power Status Register (*Table 5-52*)
0x10	r/w1c	r	BIOS Reset Source Register (*Table 5-53*)
0x11	r/w	r	Reset Mask Register (*Table 5-54*)
0x12	r/w1c	r	BIOS IPMC Watchdog Timeout Register (*Table 5-55*)
0x13	w	-	BIOS Push Button Enable Register (*Table 5-56*)
0x14	r/w1c	r	OS Reset Source Register (*Table 5-57*)
0x15	r/w1c	r	OS IPMC Watchdog Timeout Register (*Table 5-58*)
0x16	-	r/w	IPMC Watchdog Timeout Register (*Table 5-59*)
0x17	-	r/w1c	IPMC Reset Source Register (*Table 5-60*)
0x18	r/w	r	DIMM ADR Feature Configuration Register (*Table 5-62*)
0x19	-	r/w1c	IPMC Interrupt Status Register (*Table 5-61*)
0x1A	r/w1c	r	DIMM ADR Status Register (*Table 5-63*)
0x1E	-	w	CPU Control Register (*Table 5-64*)
0x1F	-	w	S-States Control Register (*Table 5-65*)
0x20	-	w	NMI Generation Register (*Table 5-66*)
0x20	r/w1c	-	NMI Interrupt Status Register (*Table 5-67*)
0x21	r/w1c	w	Internal Interrupt Status Register (*Table 5-68*)

Table 5-38 FPGA Register Map Overview (continued)

LPC Address Offset	LPC I/O	IPMC I^2C	Description
0x22	r	-	Telecom Interrupt Status Register (*Table 5-69*)
0x23	r/w	-	Telecom Interrupt Control Register (*Table 5-70*)
0x24	r	-	External Interrupt Status Register (*Table 5-71*)
0x25-0x27	r/w	-	Interrupt Mask and Map Registers (*Interrupt Mask and Map Registers on page 156*)
0x30- 0x37	r/w	r/w	CPU0 Hot Plug I^2C IO Expander Registers (*CPU0 Hot Plug I^2C IO Expander Registers on page 158*)
0x38-0x3F	r/w	r/w	CPU1 Hot Plug I^2C IO Expander Registers (*CPU1 Hot Plug I^2C IO Expander Registers on page 158*)
0x40	r	r/w	Flash Status Register (*Table 5-77*)
0x41	r/w	r	PCH Output Enable Register (*Table 5-78*)
0x42	r/w	-	RTM SPI Address/Command Register (*Table 5-79*)
0x43	r/w	-	RTM SPI Write Register (*Table 5-80*) RTM SPI Read Register (*Table 5-81*)
0x48	r/w	r	Update Channel Equalization Control Register (*Table 5-82*)
0x4A	r/w	r	RTM USB Control Register (*Table 5-83*)
0x4B	-	r	RTM Status Register (*Table 5-84*)
0x4C	-	r/w1c	RTM Interrupt Status Register (*Table 5-85*)
0x50	r/w	r	LED Control Register (*Table 5-86*)
0x52	r	r	Spare Signal Status Register (*Table 5-87*)
0x54	r	r	CPU Presence Detection Register (*Table 5-88*)
0x57	r	r	CPU Error Status Register (*Table 5-89*)
0x60	r/w	-	Telecom Clock Monitor Control Register (*Table 5-91*)
0x61	r/w1c	-	Telecom Clock Monitor Status Register (*Table 5-92*)

Table 5-38 FPGA Register Map Overview (continued)

LPC Address Offset	LPC I/O	IPMC I^2C	Description
0x62	r/w1c	-	Telecom Clock Monitor Out of Range Register (*Table 5-93*)
0x63	r/w	-	Telecom Clock Monitor Select Register (*Table 5-94*)
0x64	r/w	-	Telecom Clock Monitor Time Base Register (*Table 5-95*)
0x66-0x67	r/w	-	Telecom Clock Monitor Frequency/Period Register (*Table 5-96*)
0x68-0x69	r/w	-	Telecom Clock Monitor Lower Limit Register (*Table 5-97*)
0x6A-0x6B	r/w	-	Telecom Clock Monitor Upper Limit Register (*Table 5-98*)
0x74	r/w	r	BIOS Version Register 1 (*Table 5-99*)
0x75	r/w	r	BIOS Version Register 2 (*Table 5-100*)
0x76	r/w	r	BIOS Version Register 3 (*Table 5-101*)
0x78	r	r/w	IPMC BIOS Communication Register 1 (*Table 5-102*)
0x79	r	r/w	IPMC BIOS Communication Register 2 (*Table 5-103*)
0x7A	r	r/w	IPMC BIOS Communication Register 3 (*Table 5-104*)
0x7D	r/w	r	LPC Scratch Register (*Table 5-105*)
0x7E	r	r/w	IPMC Scratch Register (*Table 5-106*)
0x7F [1]	r/w	r	POST Code Register (*Table 5-5*)

[1] For LPC I/O address 0x80 is used. See *Table 5-5* POST Code Register.

5.1.6 Module Identification Register

The Module Identification Register identifies the ATCA-7480 blade.

Table 5-39 Module Identification Register

Address Offset: 0x00			
Bit	**Description**	**Default**	**Access**
15:0	ATCA-7480 Blade Module Identification	0x7480	r

5.1.7 Version Register

The version register provides the version of the FPGA bit stream. The initial value starts at 0x01 and will be incremented with each new release.

Table 5-40 FPGA Version Register

Address Offset: 0x02			
Bit	**Description**	**Default**	**Access**
7:0	Specifies FPGA version	0x1 (Initial Value)	r

5.1.8 Serial Redirection Control Register

BIOS sets the corresponding bit, which is used for serial redirection. The IPMC uses this information to route the corresponding port to serial IPMC interface in case of SOL.

NOTICE

BIOS should never set both status bits.

Table 5-41 Serial Redirection Control Register

Address Offset: 0x03			
Bit	**Description**	**Default**	**Access**
0	COM1 used for serial redirection: 0: COM1 not used for serial redirection 1: COM1 used for serial redirection	0	LPC: r/w IPMC: r

Table 5-41 Serial Redirection Control Register (continued)

Address Offset: 0x03			
Bit	**Description**	**Default**	**Access**
1	COM2 use for serial redirection 0: COM2 not used for serial redirection 1: COM2 used for serial redirection	0	LPC: r/w IPMC: r
7:2	Reserved	0	r

5.1.9 Serial over LAN (SOL) Control Register

The IPMC software can route serial data from serial port 1 (COM1) or serial port 2 (COM2) to the IPMC.

NOTICE

When both control bits are enabled, bit 1 is ignored.

Serial over LAN is done through NCSI from IPMC MAC to PCH. Therefore this register is implemented as backup option.

Table 5-42 Serial over LAN Control Register

Address Offset: 0x04			
Bit	**Description**	**Default**	**Access**
0	SOL over COM1 enable: 0: disabled 1: enabled. COM1 is forwarded to IMPC	PWR_GOOD: 0	IPMC: r/w LPC: r
1	SOL over COM2 enable: 0: disabled 1: enabled. COM2 is forwarded to IMPC	PWR_GOOD: 0	IPMC: r/w LPC: r
7:2	Reserved	0	r

5.1.10 Serial Line Routing Register

Table 5-43 Serial Line Routing Register

Address Offset: 0x05			
Bit	**Description**	**Default**	**Access**
0	Inverted level of signal SEL_SERIAL, which is controlled by switch SW2.1. 0: COM1 to face plate and COM2 to RTM 1: COM1 to RTM and COM2 to face plate Note: Setting may be overwritten by IPMC Software controlling Bit 4	Ext. (SW2.1) 0: OFF 1: ON	r
1	Inverted level of signal IPMC_SER_2_HEADER, which is controlled by switch SW2.2 0: IPMC Serial Debug Interface to 3 Pin Header 1: IPMC Serial Debug Interface to face plate Note: Setting may be overwritten by IPMC Software controlling Bit 5	Ext. (SW2.2) 0: OFF 1: ON	r
3:2	Reserved	0	r
4	IPMC_COM_ROUTE_A 0: COM1 to face plate and COM2 to RTM 1: COM1 to RTM and COM2 to face plate	PWR_GOOD:0	IPMC: r/w LPC: r
5	IPMC_COM_ROUTE_DEBUG 0: IPMC Serial Debug Interface to 3 Pin Header 1: IPMC Serial Debug Interface to face plate	PWR_GOOD:0	IPMC: r/w LPC: r
7:6	Reserved	0	r

5.1.11 IPMC Power Failure Registers

There are eight failure registers implemented to indicate the cause of a power failure and report some status information.

The content of the failure registers are also displayed via the seven segment LED displays.

5.1.11.1 ME Power Failure Registers

When an ME failure occurs, the red power failure LED (signal PWR_FAIL_) starts blinking. (The LED is one second ON and one second OFF).

The error state is kept until ME wakes up (signal SLP_A_ becomes high).

Table 5-44 ME Power Failure State Register

Address Offset: 0x08			
Bit	**Description**	**Default**	**Access**
2:0	ME Power Failure State. Latched last ME state when failure occurred. See *Table 5-45* ME Power Failure States. Note: Only valid with ME Failure (Bit 7) set	PWR_GOOD:0	IPMC: r
6:3	Reserved	0	IPMC: r
7	ME Failure. ME state machine sampled a failing ME Power status: 0: No ME Failure. Normal ME operation. 1: ME failure. ME failure detected.	PWR_GOOD:0	IPMC: r

The table below shows all possible failing states and their coding.

Table 5-45 ME Power Failure States

State Coding	State Name	Description
0	ME_OFF	Timeout. ASW power good for more than 45ms also ME is in ME_OFF state.
2	ME_ON:	ASW power good lost
3	ME_PWR	Timeout. No ASW power good after 45ms
4	ME_WAIT	ASW power good lost
5	ME_WAIT_OFF	ASW power good lost
Other	-	These values will never occur.

The table below shows the failing cause for the ME power failure.

Table 5-46 ME Power Failure Cause Register

Address Offset: 0x09			
Bit	**Description**	**Default**	**Access**
0	Active Sleep Well (ASW) power failure: 0: No ASW power failure. ASW power is as expected. 1: ASW power failure. ASW power has different value as expected. Note: Only valid when ME Failure (Bit 7) of ME Power Failure State Register (*Table 5-44*) is set.	PWR_GOOD:0	IPMC: r
7:1	Reserved	0	IPMC: r

5.1.11.2 Payload Power Failure Registers

When a payload power failure occurs, the red power failure LED is switched ON (signal PWR_FAIL_ is driven low).

The power failing state is kept until payload power is turned off:

- Manual Powering: Setting the switch, SW100.1 from OFF to ON.
- IPMC controlled powering: The IPMC shut down the payload power (signal IPMC_VP48_EN_ is de-asserted)

Table 5-47 Payload Power Failure State Register

Address Offset: 0x0A			
Bit	**Description**	**Default**	**Access**
4:0	Payload Power Failure State. Latched last Payload Power state when failure occurred. See *Table 5-48*. Note: Only valid with Payload Failure (Bit 7) is set.	PWR_GOOD:0	IPMC: r
6:5	Reserved	0	IPMC: r
7	Payload Power Failure. Payload Power state machine sampled a failing Payload Power status: 0: No Payload Power Failure. Normal Payload operation 1: Payload Power failure. Payload Power failure detected.	PWR_GOOD:0	IPMC: r

The table below shows all possible failing states and their coding. When the board is powered via switch SW100.1, the debug mode is enabled, where some timeouts are disabled. With debug mode enabled, the failure transition to SHUTDOWN is disabled for the states CLK_ENABLE, WAIT_100MS and S0. Nevertheless the failing state and the failing causes are latched.

Table 5-48 Payload Power Failure States

State Coding	State Name	Description
0x1	CLK_ENABLE	One or more voltages have failed, which have been already enabled and sampled good.
0x4	S0	One or more voltages have failed, which have been already enabled and sampled good. Other cause: Thermtrip
0x5	S3	One or more of these voltages have failed: 12V, 5V aux, VPP or VDD
0x7	TRACK_MASTER_ON	Timeout (debug disabled) after 280ms. Tracked voltages are not good. Other cause: 12V or 5V aux power failure
0x8	VCCIN_ENABLE	Timeout (debug disabled) after 280ms. VCCIN voltages are not good. Other cause: One or more voltages have failed, which have been already enabled and sampled good.
0x9	VCCIO_VPP_ENABLE	Timeout (debug disabled) after 280ms. VCCIO and VPP voltages are not good. Other cause: One or more voltages have failed, which have been already enabled and sampled good.
0xA	VDDQ_ENABLE	Timeout (debug disabled) after 280ms. VDD voltages are not good. Other cause: One or more voltages have failed, which have been already enabled and sampled good.
0xB	VP12_ON	Timeout (debug disabled) after 280ms. 12V or 5V aux voltages are not good.
0xC	VTT_ENABLE	Timeout (debug disabled) after 280ms. VTT voltages are not good. Other cause: One or more voltages have failed, which have been already enabled and sampled good.

Table 5-48 Payload Power Failure States (continued)

State Coding	State Name	Description
0xD	WAIT_100MS	One or more voltages have failed, which have been already enabled and sampled good.
0xE	WAKE_UP	Timeout. Board does not wake up within 5s.
Other	-	These values will never occur.

The tables below shows more details about the payload power failure. The Payload Power Failure Registers 1 to 3 content is always 0, when the Payload Power Failure status (bit 7) of Payload Power Failure State Register (*Table 5-47*) is not set.

Table 5-49 Payload Power Failure Cause Register 1

Address Offset: 0x0B			
Bit	**Description**	**Default**	**Access**
0	Payload wakeup failure: 0: No wakeup issue. Board wakes up within 5s timeout. 1: Wakeup failure. Board does not wake up (SLP_S3_ stays low) within 5s timeout	PWR_GOOD:0	IPMC: r
1	VCCIO power good failure (signal PWRGD_PVCCIO): 0: No VCCIO power issue 1: VCCIO power failure	PWR_GOOD:0	IPMC: r
6:2	Reserved	0	IPMC: r
7	Thermtrip failure (signal THERMTRIP_: 0: No Thermtrip issue 1: Thermtrip detected. THERMTRIP_ was asserted in S0 state	PWR_GOOD:0	IPMC: r

The Payload Power Failure Cause Register 2 covers the main board voltages.

Table 5-50 Payload Power Failure Cause Register 2

Address Offset: 0x0C			
Bit	**Description**	**Default**	**Access**
0	12V power good failure (signal PWRGD_VP12): 0: No 12V power issue 1: 12V power failure	PWR_GOOD:0	IPMC: r
1	5V aux power good failure (signal PWRGD_VP5AUX): 0: No 5V aux power issue 1: 5V aux power failure	PWR_GOOD:0	IPMC: r
2	5V power good failure (signal PWRGD_VP5): 0: No 5V power issue 1: 5V power failure	PWR_GOOD:0	IPMC: r
3	1.0V power good failure (signal PWRGD_V1P0): 0: No 1.0V power issue 1: 1.0V power failure	PWR_GOOD:0	IPMC: r
4	0.75V power good failure (signal PWRGD_V0P75): 0: No 0.75V power issue 1: 0.75V power failure	PWR_GOOD:0	IPMC: r
5	3.3V and 1.05V power good failure (signal PWRGD_V3P3_V1P05): 0: No 3.3V and 1.05 power issue 1: 3.3V and 1.05 power failure	PWR_GOOD:0	IPMC: r
6	1.8V power good failure (signal PWRGD_V1P8): 0: No 1.8V power issue 1: 1.8V power failure	PWR_GOOD:0	IPMC: r
7	1.5V power good failure (signal PWRGD_V1P5): 0: No 1.5V power issue 1: 1.5V power failure	PWR_GOOD:0	IPMC: r

The Payload Power Failure Cause Register 3 covers CPU specific voltages. When a CPU is not mounted (detected via CPU0_SKTOCC_ and CPU1_SKTOCC_), the corresponding power failure bits will never be set.

Table 5-51 Payload Power Failure Cause Register 3

Address Offset: 0x0D			
Bit	**Description**	**Default**	**Access**
0	VPP CPU0 power good failure (signal PWRGD_PVPP_ABCD): 0: No VPP CPU0 power issue 1: VPP CPU0 power failure	PWR_GOOD:0	IPMC: r
1	VPP CPU1 power good failure (signal PWRGD_PVPP_EFGH): 0: No VPP CPU1 power issue 1: VPP CPU1 power failure	PWR_GOOD:0	IPMC: r
2	VDD CPU0 power good failure (signal PWRGD_VDD_ABCD): 0: No VDD CPU0 power issue 1: VDD CPU0 power failure	PWR_GOOD:0	IPMC: r
3	VDD CPU1 power good failure (signal PWRGD_VDD_EFGH): 0: No VDD CPU1 power issue 1: VDD CPU1 power failure	PWR_GOOD:0	IPMC: r
4	VTT CPU0 power good failure (signal PWRGD_VTT_ABCD): 0: No VTT CPU0 power issue 1: VTT CPU0 power failure.	PWR_GOOD:0	IPMC: r
5	VTT CPU1 power good failure (signal PWRGD_VTT_EFGH): 0: No VTT CPU1 power issue 1: VTT CPU1 power failure	PWR_GOOD:0	IPMC: r
6	VCCIN CPU0 power good failure (signal PWRGD_PVCCIN_CPU0): 0: No VCCIN CPU0 power issue 1: VCCIN CPU0 power failure	PWR_GOOD:0	IPMC: r

Table 5-51 Payload Power Failure Cause Register 3 (continued)

Address Offset: 0x0D			
Bit	**Description**	**Default**	**Access**
7	VCCIN CPU1 power good failure (signal PWRGD_PVCCIN_CPU1): 0: No VCCIN CPU1 power issue 1: VCCIN CPU1 power failure	PWR_GOOD:0	IPMC: r

5.1.11.3 Power Status Register

This register provides some status information of external signals connected to the FPGA. The content corresponds to the external signal level.

Table 5-52 Power Status Register

Address Offset: 0x0E			
Bit	**Description**	**Default**	**Access**
0	Status of signal SLP_A_.	Ext.	IPMC: r
1	Status of signal SLP_S4_.	Ext.	IPMC: r
2	Status of signal SLP_S3_.	Ext.	IPMC: r
3	Reserved	0	IPMC: r
4	Status of signal CPU_PWRGD	Ext.	IPMC: r
5	Status of signal XDP_HOOK1_SEL	Ext.	IPMC: r
6	Status of signal XDP_PWRGD_RST_	Ext.	IPMC: r
7	Status of signal XDP_CPU_SYSPWROK	Ext.	IPMC: r

5.1.12 Reset Registers

5.1.12.1 BIOS Reset Source Register

The BIOS Reset Source Register stores the source of the most recent reset. A “1” in the register bit indicates that the associated reset has occurred. If more than one reset occurs from different sources without clearing the corresponding register bits, one cannot determine the most recent reset source since more than one bit will be set. The same situation will happen if two reset sources go active at the same time.

NOTICE

OS should never write to this register.

Table 5-53 BIOS Reset Source Register

Address Offset: 0x10			
Bit	**Description**	**Default**	**Access**
0	PWR_GOOD Payload Power-on reset 1: Reset occurred	PWR_GOOD:1	LPC: r/w1c IPMC: r
1	XDPx reset request (Any one of XDPx signal caused reset 1: Reset occurred	PWR_GOOD:0	LPC: r/w1c IPMC: r
2	PB_RST_ face plate push button reset 1: Reset occurred	PWR_GOOD:0	LPC: r/w1c IPMC: r
3	Reserved	0	r
4	RTM_PB_RST_ Reset key at RTM 1: Reset occurred	PWR_GOOD:0	LPC: r/w1c IPMC: r
5	Reserved	0	r
6	PCH_PLTRST_ reset 1: Reset occurred	PWR_GOOD:0	LPC: r/w1c IPMC: r
7	IPMC_RST_ REQ_ Payload Reset from IPMC. 1: Reset occurred	PWR_GOOD:0	LPC: r/w1c IPMC: r

5.1.12.2 Reset Mask Register

The reset mask register enables or disables forwarding of a reset source to reset output signal. Only Push Button Resets requests are masked using the reset mask register. The register default values are latched when PWR_GOOD is asserted. This register can be read or written by the host CPU. A “1” in the register bit indicates that the associated reset is enabled. A “0” indicates that the associated reset source is masked.

Table 5-54 Reset Mask Register

Address Offset: 0x11			
Bit	**Description**	**Default**	**Access**
1:0	Reserved	0	r
2	PB_RST_ face plate push button reset 1: enabled 0: disabled	Ext.: FACE_PB_EN 1: (SW2.4 is OFF) 0: (SW2.4 is ON)	LPC: r/w
3	Reserved	0	r
4	RTM_PB_RST_ Reset key at RTM 1: enabled 0: disabled	Ext.: FACE_PB_EN 1: (SW2.4 is OFF) 0: (SW2.4 is ON)	LCP: r/w
7:5	Reserved	0	r

5.1.12.3 BIOS IPMC Watchdog Timeout Register

When one of the IPMC Watchdog Timeout bit of IPMC Watchdog Timeout Register is set, the corresponding BIOS IPMC Watchdog Timeout bit is set. The BIOS clears this status bit by writing one.

NOTICE

OS should never write to this register.

Table 5-55 BIOS IPMC Watchdog Timeout Register

Address Offset: 0x12			
Bit	**Description**	**Default**	**Access**
0	BIOS IPMC Watchdog Timeout: 1: IPMC Watchdog Timeout occurred	PWR_GOOD:0	LPC: r/w1c IPMC: r
1	BIOS IPMC Pre-Timeout 1: IPMC Pre-Timeout occurred	PWR_GOOD:0	LPC: r/w1c IPMC: r
7:2	Reserved	0	r

5.1.12.4 BIOS Push Button Enable Register

The BIOS needs to write to this register to enable the Front Panel push button reset, the RTM push button reset and the IPMC reset.

NOTICE

After a timeout of 8s, the resets are armed again.

Table 5-56 BIOS Push Button Enable Register

Address Offset: 0x13			
Bit	**Description**	**Default**	**Access**
7:0	BIOS Push Button Enable Register	-	LPC: w

5.1.12.5 OS Reset Source Register

The OS Reset Source Register stores the source of the most recent reset. It is similar to the BIOS Reset Source Register. A “1” in the register bit indicates that the associated reset has occurred. If more than one reset occurs from different sources without clearing the corresponding register bits, one cannot determine the most recent reset source since more than one bit will be set. The same will happen if two reset sources go active at the same time.

NOTICE

BIOS should never write to this register.

Table 5-57 OS Reset Source Register

Address Offset: 0x14			
Bit	**Description**	**Default**	**Access**
0	PWR_GOOD Payload Power-on reset 1: Reset occurred	PWR_GOOD:1	LPC: r/w1c IPMC: r
1	XDPx reset request (Any one of XDPx signal caused reset 1: Reset occurred	PWR_GOOD:0	LPC: r/w1c IPMC: r
2	PB_RST_ face plate push button reset 1: Reset occurred	PWR_GOOD:0	LPC: r/w1c IPMC: r
3	Reserved	0	r
4	RTM_PB_RST_ Reset key at RTM 1: Reset occurred	PWR_GOOD:0	LPC: r/w1c IPMC: r
5	Reserved	0	r
6	PCH_PLTRST_ reset 1: Reset occurred	PWR_GOOD:0	LPC: r/w1c IPMC: r
7	IPMC_RST_ REQ_ Payload Reset from IPMC. 1: Reset occurred	PWR_GOOD:0	LPC: r/w1c IPMC: r

5.1.12.6 OS IPMC Watchdog Timeout Register

When one of the IPMC Watchdog Timeout bits of IPMC Watchdog Timeout Register is set, the corresponding OS IPMC Watchdog Timeout Register bit is set. The OS clears this status bit by writing one.

NOTICE

BIOS should never write to this register.

Table 5-58 OS IPMC Watchdog Timeout Register

Address Offset: 0x15			
Bit	**Description**	**Default**	**Access**
0	OS IPMC Watchdog Timeout: 1: IPMC Watchdog Timeout occurred	PWR_GOOD:0	LPC: r/w1c IPMC: r
1	OS IPMC Pre-Timeout 1: IPMC Pre-Timeout occurred	PWR_GOOD:0	LPC: r/w1c IPMC: r
7:2	Reserved	0	r

5.1.12.7 IPMC Watchdog Timeout Register

The IPMC SW sets the corresponding bit to signal of an IPMC watchdog timeout event. When the IPMC Watchdog Timeout bit is set from low to high, the corresponding bits in *Table 5-55* and *Table 5-58* are set.

NOTICE

IPMC needs to clear the IPMC watchdog timeout bit to arm IPMC watchdog timeout event recognition.

Table 5-59 IPMC Watchdog Timeout Register

Address Offset: 0x16			
Bit	**Description**	**Default**	**Access**
0	IPMC Watchdog Timeout: 0: No IPMC Watchdog Timeout 1: IPMC Watchdog Timeout occurred	PWR_GOOD:0	IPMC: r/w
1	IPMC Pre-Timeout 0: No IPMC Pre-Timeout 1: IPMC Pre-Timeout occurred	PWR_GOOD:0	IPMC: r/w
7:2	Reserved	0	r

5.1.12.8 IPMC Reset Source Register

The IPMC Reset Source Register stores the source of the most recent reset. A “1” in the register bit indicates that the associated reset has occurred. If more than one reset occurs from different sources without clearing the corresponding register bits, one cannot determine the most recent reset source since more than one bit will be set. The same situation will happen if two reset sources go active at the same time.

Table 5-60 IPMC Reset Source Register

Address Offset: 0x17			
Bit	**Description**	**Default**	**Access**
0	PWR_GOOD Payload Power-on reset 1: Reset occurred	PWR_GOOD:1	IPMC: r/w1c
1	XDPx reset request (Any one of XDPx signal caused reset 1: Reset occurred	PWR_GOOD:0	IPMC: r/w1c
2	PB_RST_ face plate push button reset 1: Reset occurred	PWR_GOOD:0	IPMC: r/w1c
3	Reserved	0	r
4	RTM_PB_RST_ Reset key at RTM 1: Reset occurred	PWR_GOOD:0	IPMC: r/w1c
5	Reserved	0	r
6	PCH_PLTRST_ reset 1: Reset occurred	PWR_GOOD:0	IPMC: r/w1c
7	IPMC_RST_ REQ_ Payload Reset from IPMC. 1: Reset occurred	PWR_GOOD:0	IPMC: r/w1c

5.1.12.9 IPMC Interrupt Status Register

The IPMC Interrupt Status Register stores the IPMC interrupt event. The event is cleared by IMPC with write one to clear.

NOTICE

IPMC version 1.2.0018 or higher is needed to clear the interrupt flag. Otherwise the IPMC interrupt will always be active and produce infinite IPMC interrupts.

Table 5-61 IPMC Interrupt Status Register

Address Offset: 0x19			
Bit	**Description**	**Default**	**Access**
0	IPMC interrupt status 1: Platform Reset occurred (PCH_PLT_RST_)	PWR_GOOD:0	IPMC: r/w1c
7:1	Reserved	0	r

5.1.12.10 DIMM ADR Configuration Register

The DIMM ADR Configuration Register enables or disables the ADR feature. Each bit of this register corresponds to a reset source. When a bit is set, it enables the ADR for the corresponding reset signal. Upon receiving a reset event, FPGA reset logic looks if the ADR is enabled for that particular reset. When enabled, PCH_ADR_IRQ_ signal is asserted. When PCH signals completion with assertion of ADR_COMPLETE the Reset State Machine asserts PCH_SYS_RST_. If ADR is not enabled PCH_SYS_RST_ is generated immediately without the assertion of PCH_ADR_IRQ_ signal.

Table 5-62 DIMM ADR Feature Configuration Register

Address Offset: 0x18			
Bit	**Description**	**Default**	**Access**
0	ADR enable for Push button reset 1: ADR enabled 0: ADR disabled	PWR_GOOD:0	LPC: r/w IPMC: r
1	ADR enable for RTM Push button reset 1: ADR enabled 0: ADR disabled	PWR_GOOD:0	LPC: r/w IPMC: r
2	ADR enable for IPMI reset 1: ADR enabled 0: ADR disabled	PWR_GOOD:0	LPC: r/w IPMC: r
7:3	Reserved	0	r

5.1.12.11 DIMM ADR Status Register

BIOS can read the status of PCH_ADR_IRQ_ signal from this register on boot up. This gives BIOS the information that the DIMM has data stored from last boot. BIOS must clear this register after boot up. Writing “1” to this register bit clears the register bit.

Table 5-63 DIMM ADR Status Register

Address Offset: 0x1A			
Bit	**Description**	**Default**	**Access**
0	Indicates if the ADR feature is enabled. (GPIO37 of Cavecreek) 0: ADR disabled (PCH_ADR_IRQ_ is driven high) 1: ADR enabled (PCH_ADR_IRQ_ is driven low)	PWR_GOOD:0	LPC: r/w1c IPMC: r
7:1	Reserved	0	r

5.1.13 CPU Control Register

Table 5-64 CPU Control Register

Address Offset: 0x1E			
Bit	**Description**	**Default**	**Access**
0	PCH_PSTATE_ pulse generation. Minimum low pulse width is Xµs 0: No action 1: Generate PSTATE low pulse.	-	IPMC: w
1	PCH_RCIN_ pulse generation. Minimum low pulse width is Xµs: 0: No action 1: Generate RCIN low pulse.	-	IPMC: w
7:2	Reserved	-	-

5.1.14 S-States Control Register

IPMC can initiate S-State transitions:

- S0 to S3. Triggered with SIC low pulse
- S3, S4 or S5 to S0: Triggered with short PWRBTN low pulse

- S0 to S5: Trigger graceful Shutdown with short PWRBTN low pulse
- S0 to S5: Trigger forced Shutdown with long PWRBTN low pulse

Table 5-65 S-States Control Register

Address Offset: 0x1F			
Bit	**Description**	**Default**	**Access**
0	SCI pulse generation. Minimum low pulse width is 45ms: 0: No action 1: Generate SCI low pulse. Trigger S0 -> S3 transition	-	IPMC: w
1	PWRBTN pulse generation. Minimum low pulse width is 32ms: 0: No action 1: Generate PWRBTN low pulse. Trigger S3/S5 -> S0 transition or when in S0 a “graceful” shutdown is triggered.	-	IPMC: w
2	Power Button Override Function. PWRBTN low pulse is 5s. 0: No action 1: Generate PWRBTN long low pulse. Forced transition to S5	-	IPMC: w
7:3	Reserved	-	-

5.1.15 NMI Control Status Registers

IPMC can initiate a NMI. Host can identify NMI comes from IPMC.

5.1.15.1 NMI Generation Register

IPMC can initiate a NMI high pulse writing 0xA5 to this register. The minimum pulse width of the NMI is 175µs.

Table 5-66 NMI Generation Register

Address Offset: 0x20			
Bit	**Description**	**Default**	**Access**
7:0	NMI pulse generation. Minimum pulse width is 175µs: 0xA5: Generate NMI pulse all other values are ignored	-	IPMC: w

5.1.15.2 NMI Interrupt Status Register

When the IPMC has generated a NMI pulse, the host can identify this event reading the register below. The host needs to clear this flag.

Table 5-67 NMI Interrupt Status Register

Address Offset: 0x20				
Bit	**Signal/ Group**	**Description**	**Default**	**Access**
0	PCH_NMI	NMI pulse triggered by IPMC.	PWR_GOOD: 0	LPC: r/1wc
7:1	-	Reserved	0	r

5.1.16 Interrupt Control and Status Registers

The interrupt status registers indicate events of the interrupt input signals. When an interrupt event occurred, the corresponding status bit is read 1. Writing 1 of the corresponding bit clears the bit.

5.1.16.1 Internal Interrupt Status Register

Table 5-68 Internal Interrupt Status Register

Address Offset: 0x21			
Bit	**Description**	**Default**	**Access**
0	IPMC signals interrupt. Host clears flag.	0	LPC: r/1wc
	IPMC generates host interrupt: 0: no action 1: generate minimum 175µs interrupt pulse	-	IPMC: w
7:1	Reserved	0	r

5.1.16.2 Telecom Interrupt Status Register

This register reflects the status of telecom related interrupt signals. The corresponding Telecom interrupt sources need to be enabled. Use of this register is optional, because the same information can be found at: *Table 5-92* and *Table 5-93*. These tables also show how to clear the corresponding interrupt status bits.

Table 5-69 Telecom Interrupt Status Register

Address Offset: 0x22			
Bit	**Description**	**Default**	**Access**
3: 0	Telecom CLK_MONITOR_FINISHED interrupt: One or more Telecom Clock measurements have finished.	-	LPC: r
7:4	Telecom CLK_MONITOR_OUT_OF_RANGE interrupt: One or more Telecom Clocks are out of range	-	LPC: r

5.1.16.3 Telecom Interrupt Control Register

Each of the Telecom interrupt source can be enabled.

Table 5-70 Telecom Interrupt Control Register

Address Offset: 0x23			
Bit	**Description**	**Default**	**Access**
3: 0	Telecom CLK_MONITOR_FINISHED interrupt enable: Enable/Disable interrupt for the corresponding Clock source: 0: interrupt is disabled 1: Interrupt is enabled	0	LPC: r/w
7:4	Telecom CLK_MONITOR_OUT_OF_RANGE interrupt: Enable/Disable interrupt for the corresponding Clock source: 0: interrupt is disabled 1: Interrupt is enabled	0	LPC: r/w

5.1.16.4 RTM Interrupt Status Register

The RTM Interrupt Status Register will be located in the RTM SPI address space. The host can access the RTM register using the RTM SPI Master Interface.

5.1.16.5 External Interrupt Status Register

Table 5-71 External Interrupt Status Register

Address Offset: 0x24				
Bit	**Signal/Group**	**Description**	**Default**	**Access**
0	RTM_SPI_MISO	RTM interrupt sources 0: RTM_SPI_MISO is high. No RTM interrupt. 1: RTM_SPI_MISO is low. One or more RTM interrupt sources are active. When RTM SPI Master face is active the current level is latched.	Ext.	LPC: r
7:1	-	Reserved	0	r

5.1.16.6 Interrupt Mask and Map Registers

Interrupts from different interrupt sources including the External Interrupt sources can be mapped to any IRQ Frame number of the serialized IRQ protocol.

Multiple interrupt sources may share the same IRQ Frame. In this case all interrupt sources need to be of type “level active low”.

Each interrupt source has an Interrupt Mask and Map Register. See *Table 5-72*.

Table 5-72 Address Map of Interrupt Mask and Map Registers

Interrupt Source(s)	**Description**	**Address Offset of Interrupt Mask**
IPMC to Host Interrupt	IPMC signals interrupt	0x25
Telecom Interrupt	Telecom Interrupt	0x26
RTM_SPI_MISO	RTM interrupt sources	0x27

Each Interrupt Mask and Map Register has the same layout. See *Table 5-73* for more details.

Table 5-73 Interrupt Mask and Map Registers

Address Offset: 0x25 - 0x27			
Bit	**Description**	**Default**	**Access**
4:0	IRQ Frame Number of Serialized IRQ protocol. Any valid Frame number enables interrupt. 0x00: Interrupt is disabled. 0x01: Frame number 1. IRQ0 0x02: Frame number 2. IRQ1 0x03: Frame number 3. IRQ2 (SMI_) 0x04: Frame number 4. IRQ3 0x05: Frame number 5. IRQ4 0x06: Frame number 6. IRQ5 0x07: Frame number 7. IRQ6 0x08: Frame number 8. IRQ7 0x09: Frame number 9. IRQ8 0x0A: Frame number 10. IRQ9 0x0B: Frame number 11. IRQ1 0x0C: Frame number 12. IRQ11 0x0D: Frame number 13. IRQ12 0x0E: Frame number 14. IRQ13 0x0F: Frame number 15. IRQ14 0x10: Frame number 16. IRQ15 0x11: Frame number 17. IOCHK_ 0x12: Frame number 18. INTA_ 0x13: Frame number 19. INTB_ 0x14: Frame number 20. INTC_ 0x15: Frame number 21. INTD_ 0x16 - 0x1F: Frame number 22-31. IRQ Frame Number not valid. Value is ignored.	0	LPC: r/w
7:5	Reserved	0	r

5.1.17 PCI Express Hot Plug I2C IO Expander Registers

Each CPU supports four PCI Express Hot Plug ports.

5.1.17.1 CPU0 Hot Plug I2C IO Expander Registers

The Hot Plug registers for CPU0 are mapped to 0x30 to 0x37

5.1.17.2 CPU1 Hot Plug I2C IO Expander Registers

The Hot Plug registers for CPU1 are mapped to 0x38 to 0x3F.

5.1.17.3 Hot-Plug Virtual Pin Port Registers

Each Port has a Hot Plug Interface, which can be accessed by the Hot-Plug Virtual Pin Port Register (see *Table 5-74*).

Table 5-74 Hot-Plug Virtual Pin Port Register

Address Offset: **CPU0: Port 1: 0x30,Port 2: 0x31, Port 3: 0x32, Port 4: 0x33** **CPU1: Port 1: 0x38,Port 2: 0x39, Port 3: 0x3A, Port 4: 0x3B**					
Bit	**Signal Name**	**Direction**	**Description**	**Default**	**Access**
0	ATNLED	Output	This indicator is connected to the Attention LED on the baseboard. For a precise definition refer to PCI Express Base Specification, Revision 3.0.	Ext.	r
1	PWRLED	Output	This indicator is connected to the Power LED on the baseboard. For a precise definition refer to PCI Express Base Specification, Revision 3.0.	Ext.	r
2	PWREN#	Output	Output signal allowing software to enable or disable power to a PCI Express slot.	Ext.	r
3	BUTTON#	Input	Input signal per slot which indicates that the user wishes to hot remove or hot add a PCI Express card/module.	1	IPMC: r/w LPC: r

Table 5-74 Hot-Plug Virtual Pin Port Register (continued)

Address Offset: **CPU0: Port 1: 0x30,Port 2: 0x31, Port 3: 0x32, Port 4: 0x33** **CPU1: Port 1: 0x38,Port 2: 0x39, Port 3: 0x3A, Port 4: 0x3B**					
Bit	**Signal Name**	**Direction**	**Description**	**Default**	**Access**
4	PRSNT#	Input	Input signal that indicates if a hot pluggable PCI Express card/module is currently plugged into the slot.	1	IPMC: r/w LPC: r
5	PWRFLT#	Input	Input signal from the power controller to indicate that a power fault has occurred.	1	IPMC: r/w LPC: r
6	MRL#/ EMILS	Input	Manual retention latch status or Electromechanical latch status input indicates that the retention latch is closed or open. Manual retention latch is used on the platform to mechanically hold the card in place and can be open/closed manually. Electromechanical latch is used to electro-mechanically hold the card in place and is operated by software. MRL# is used for card-edge and EMLSTS# is used for SIOM form-factors.	1	IPMC: r/w LPC: r
7	EMIL	Output	Electromechanical retention latch control output that opens or closes the retention latch on the board for this slot. A retention latch is used on the platform to mechanically hold the card in place. Refer to PCI Express Server/Workstation Module Electromechanical Spec Rev 1.0 for details of the timing requirements of this pin output.	Ext.	r

5.1.17.4 PCA9555 Internal Register access

For debug purpose the internal virtual PCA9555 registers can be read by the IPMC and the Service Processor.

Table 5-75 Address Control for PCA9555 Internal Register

Address Offset: **CPU0 Device1 (Slave address 0x20): 0x34** **CPU0 Device2 (Slave address 0x21): 0x36** **CPU1 Device1 (Slave address 0x20): 0x3C** **CPU1 Device1 (Slave address 0x21): 0x3E**			
Bit	**Description**	**Default**	**Access**
2:0	Internal PCA9555 register address	0	r/w
7:3	Reserved	0	r

Table 5-76 Content of PCA9555 Internal Register

Address Offset: **CPU0 Device1 (Slave address 0x20): 0x35** **CPU0 Device2 (Slave address 0x21): 0x37** **CPU1 Device1 (Slave address 0x20): 0x3D** **CPU1 Device1 (Slave address 0x21): 0x3F**			
Bit	**Description**	**Default**	**Access**
7:0	Content of PCA9555 register	0	r

5.1.18 Flash Status and Selection Registers

The flash status register indicates the actual status of the mechanical switches SW1.3 (Signal BOOT_TSOP), SW3.1 (Signal BOOT_SEL_EN_) and SW3.2 (Signal BOOT_DEFAULT).

The register also provides information about the actual Boot Flash selection (status bit CURRENT_BOOT_SELECT) and the IPMC selected Boot Flash (status bit TARGET_BOOT_SELECT).

The IPMC Target Boot Flash selection will become active with next platform reset. When the bits, TARGET_BOOT_SELECT and CURRENT_BOOT_SELECT are different, an alternate BIOS needs to be selected. In this case the platform reset will be transformed by the FPGA logic to payload power cycle including the ME. This is done to guarantee no SPI access to boot flash when switching the other device.

Table 5-77 Flash Status Register

Address Offset: 0x40			
Bit	**Description**	**Default**	**Access**
0	CURRENT_BOOT_SELECT: Current Boot Flash selection. Is valid until next platform reset.	0	r
3:1	Reserved	0	r
4	TSOP or PLCC Boot select. Signal BOOT_TSOP. 0: TSOP selected 1: PLCC selected	Ext. 0: SW1.3 OFF 1: SW1.3 ON	r
5	Manual Boot Flash select enable. Signal BOOT_SEL_EN_. 0: Signal BOOT_SELECT selects active boot flash 1: Switch SW3.2 selects the active Boot Flash.	Ext. 0: SW3.1 OFF 1: SW3.1 ON	r
6	Manual Boot Flash select. Signal BOOT_DEFAULT. Used when SW3.1 is ON: 0: Selects Default Boot SPI Flash. 1: Selects Recover Boot SPI Flash.	Ext. 0: SW3.2 OFF 1: SW3.2 ON	r
7	TARGET_BOOT_SELECT. Target Boot Flash Selection. 0: Selects Default Boot SPI Flash 1: Selects Recovery Boot SPI Flash Note: New flash selection valid with next platform reset	PWR_GOOD: 0	LPC: r IPMC: r/w

5.1.19 PCH Output Enable Register

The output signals, PCH_RCIN_, PCH_SCI_ and PCH_PSTATE_ are connected to the GPIO Pins of the PCH. After power-up, the PCH drives these signals. To avoid signal contention, the outputs are tri-stated. After software has configured the PCH GPIO pins as inputs, the corresponding outputs can be enabled with this Register.

Table 5-78 PCH Output Enable Register

Address Offset: 0x41			
Bit	**Description**	**Default**	**Access**
0	PCH_RCIN_ enable: 0: Disabled. Signal is tri-state 1: Enabled. Drive pch_rcin	0	LPC: r/w
1	PCH_SCI_ enable: 0: Disabled. Signal is tri-state 1: Enabled. Drive pch_sci	0	LPC: r/w
2	PCH_PSTATE_ enable: 0: Disabled. Signal is tri-state 1: Enabled. Drive pch_pstate	0	LPC: r/w
7:3	Reserved	0	0

5.1.20 RTM SPI Interface Registers

The signals, RTM_SPI_SCK, RTM_SPI_SS_, RTM_SPI_MISO and RTM_SPI_MOSI are used to support a SPI master protocol. The signal, RTM_SPI_MISO is also used to signal an ARTM interrupt to the base board. See Chapter 5.18.4 RTM Interrupt Status Register.

NOTICE

At the moment there is no ARTM with an SPI interface defined.

A write access to the RTM SPI Address/Command Register starts the SPI transaction. The write cycle terminates when SPI transaction is finished.

Table 5-79 RTM SPI Address/Command Register

Address Offset: 0x42			
Bit	**Description**	**Default**	**Access**
0	Command Bit 0: Write 1: Read	0	LPC: r/w
7:1	RTM SPI Address bits [6:0]	0	LPC: r/w

A write access to the RTM SPI Address/Command Register with the Command Bit 0 (Write) starts a SPI write transaction. The data byte in the SPI Write Register is written to the SPI device.

Table 5-80 RTM SPI Write Register

Address Offset: 0x43			
Bit	**Description**	**Default**	**Access**
7:0	RTM SPI write data	-	LPC: w

A write access to the RTM SPI Address/Command Register with the Command Bit 1 (Read) starts a SPI read transaction. This contains the data read from the SPI device.

Table 5-81 RTM SPI Read Register

Address Offset: 0x43			
Bit	**Description**	**Default**	**Access**
7:0	RTM SPI read data	0	LPC: r

5.1.21 Update Channel Equalization Control Register

Table 5-82 Update Channel Equalization Control Register

Address Offset: 0x48			
Bit	**Description**	**Default**	**Access**
0	Control output Signal UC1_EQ_RX: 0: UC1_EQ_RX is driven low 1: UC1_EQ_RX is tri-state	0	LPC: r/w IPMC: r
1	Control output Signal UC1_EQ_TX: 0: UC1_EQ_TX is driven low 1: UC1_EQ_TX is tri-state	0	LPC: r/w IPMC: r
2	Control output Signal UC2_EQ_RX: 0: UC2_EQ_RX is driven low 1: UC2_EQ_RX is tri-state	0	LPC: r/w IPMC: r
3	Control output Signal UC2_EQ_TX: 0: UC2_EQ_TX is driven low 1: UC2_EQ_TX is tri-state	0	LPC: r/w IPMC: r
4	Control output Signal UC3_EQ_RX: 0: UC3_EQ_RX is driven low 1: UC3_EQ_RX is tri-state	0	LPC: r/w IPMC: r
5	Control output Signal UC3_EQ_TX: 0: UC3_EQ_TX is driven low 1: UC3_EQ_TX is tri-state	0	LPC: r/w IPMC: r
6	Control output Signal UC4_EQ_RX: 0: UC4_EQ_RX is driven low 1: UC4_EQ_RX is tri-state	0	LPC: r/w IPMC: r
7	Control output Signal UC4_EQ_TX: 0: UC4_EQ_TX is driven low 1: UC4_EQ_TX is tri-state	0	LPC: r/w IPMC: r

5.1.22 RTM USB Control Register

Table 5-83 RTM USB Control Register

Address Offset: 0x4A			
Bit	**Description**		**Access**
0	Reserved	0	r
1	Disable/Enable USB Port 2 to RTM. 0: RTMUSB_ENABLE_ driven low. Enabled 1: RTMUSB_ENABLE_ driven high. Disabled	PWR_GOOD: 1	LPC: r/w IPMC: r
7:2	Reserved	0	r

Table 5-84 RTM Status Register

Address Offset: 0x4B			
Bit	**Description**	**Default**	**Access**
0	RTM power good status: 0: RTM power not stable or RTM not powered 1: RTM power good	Ext: RTM_PWRGD	IPCM: r
7:1	Reserved	0	IPCM: r

Table 5-85 RTM Interrupt Status Register

Address Offset: 0x4C			
Bit	**Description**	**Default**	**Access**
0	Face plate Ethernet 1 Interrupt (signal PV_FPETH_1_INT_): 0: No interrupt 1: Interrupt detected (falling edge PV_FPETH_1_INT_)	0	IPCM: r/w1c
1	Base Ethernet 1 Interrupt (signal PV_BASE_1_INT_): 0: No interrupt 1: Interrupt detected (falling edge PV_BASE_1_INT_)	0	IPCM: r/w1c
7:2	Reserved	0	IPMC: r

5.1.23 LED Status and Control Register

Table 5-86 LED Control Register

Address Offset: 0x50			
Bit	**Description**	**Default**	**Access**
0	Control green LED output Signal LED_GREEN_: 0: LED_GREEN_ is driven high. LED off 1: LED_GREEN_ is driven low. LED on	0	r/w
1	Control read LED output Signal LED_RED_: 0: LED_RED_ is driven high. LED off 1: LED_RED_ is driven low. LED on	0	r/w
2	Control user LED output Signal LED_USER1_: 0: LED_USER1_ is driven high. LED off 1: LED_USER1 is driven low. LED on	0	r/w
3	Control user LED output Signal LED_USER2_: 00: LED_USER2_ is driven high. LED off 01: LED_USER2 is driven low. LED on	0	r/w
7:4	Reserved	0	r

5.1.24 Spare Signals Status Registers

Table 5-87 Spare Signal Status Register

Address Offset: 0x52			
Bit	**Description**	**Default**	**Access**
0	Signal level of SW100_2 (Connected to SW100.2)	Ext.	r
1	Signal level of SW1.4 (Connected to SW1.4)	Ext.	r
3:2	Signal level of spare connections SPARE[2:1]	Ext.	r
7:4	Reserved	Ext.	r

5.1.25 CPU Presence Detection Register

Table 5-88 CPU Presence Detection Register

Address Offset: 0x54			
Bit	**Description**	**Default**	**Access**
1:0	Reserved	0	r
2	CPU0 Presence Detection (Status of signal CPU0_SKTOCC_) 0: CPU present in socket 1: CPU not present. Socket is empty	Ext.	r
3	CPU1 Presence Detection (Status of signal CPU1_SKTOCC_) 0: CPU present in socket 1: CPU not present. Socket is empty	Ext.	r
7:4	Reserved	0	r

5.1.26 CPU Error Status Register

Table 5-89 CPU Error Status Register

Address Offset: 0x57				
Bit	**Signal**	**Description**	**Default**	**Access**
0	CPU_ERR_[0]	CPU Error status signals. Bit 0 = Non critical Error Bit 1 = Non-fatal error (operating system or firmware action required to contain and recover) Bit 2 = Fatal error (system reset likely required to recover)	Ext.	r
1	CPU_ERR_[1]		Ext.	r
2	CPU_ERR_[2]		Ext.	r
7:3	-	Reserved	0	r

5.1.27 Telecom Clock Supervision Registers

All incoming telecom clocks can be monitored and measured in the range from 1 Hz to 166 MHz. Up to 4 different clock inputs may be monitored. See table below.

Table 5-90 Supervised Telecom Clocks Reference List

Number	Name	Description
0	SYSCLK_IN_CLK1A	CLK1A from backplane
1	SYSCLK_IN_CLK1B	CLK1B from backplane
2	SYSCLK_IN_CLK2A	CLK2A from backplane
3	SYSCLK_IN_CLK2B	CLK2B from backplane

Table 5-91 Telecom Clock Monitor Control Register

Address: 0x60			
Bit	**Description**	**Default**	**Access**
3:0	Enable supervised Telecom Clock 0 to 3 Set corresponding bit enable monitoring.	0	LPC: r/w
7:4	Reserved	0	r

When at least one bit of the *Table 5-91* is set, the corresponding status bit CLK_MONITOR_FINISHED of the *Table 5-69* is also set.

Table 5-92 Telecom Clock Monitor Status Register

Address: 0x61			
Bit	**Description**	**Default**	**Access**
3:0	Result available for supervised Telecom Clock 0 to 3. Corresponding bit is set when measurement has finished. Clearing bit triggers new measurement.	0	LPC: r/w1c
7:4	Reserved	0	r

When at least one bit of the *Table 5-93* is set, the corresponding status bit CLK_MONITOR_OUT_OF_RANGE of *Table 5-69* is also set.

Table 5-93 Telecom Clock Monitor Out of Range Register

Address: 0x62			
Bit	**Description**	**Default**	**Access**
3:0	Frequency of supervised Telecom Clock 0 to 3 is out of range. Gate Mode: Corresponding bit is set when the number of positive Clock edges within the selected time base is: < Lower limit or > Upper limit Period Mode: Corresponding bit is set when the Clock 0 Period within the selected time base is: < Lower limit or > Upper limit Clearing bit triggers new sequence of measurements.	0	LPC: r/w1c
7:4	Reserved	0	r

Table 5-94 Telecom Clock Monitor Select Register

Address: 0x63			
Bit	**Description**	**Default**	**Access**
1:0	Select supervised Telecom Clocks. See *Table 5-90* Supervised Telecom Clocks Reference List: 0-3: Select corresponding clock.	0	LPC: r/w
7:2	Reserved	0	r

The following tables refer to the clock selected with *Table 5-94*.

Table 5-95 Telecom Clock Monitor Time Base Register

Address: 0x64			
Bit	**Description**	**Default**	**Access**
4:0	Select Time base for clock supervision with Gate Mode: 0: Gate is open for 250µs 1: Gate is open for 500µs 2: Gate is open for 1ms 3: Gate is open for 2ms 4: Gate is open for 4ms 5: Gate is open for 8ms 6: Gate is open for 16ms 7: Gate is open for 32ms 8: Gate is open for 64ms 9: Gate is open for 128ms 10: Gate is open for 256ms 11: Gate is open for 512ms 12: Gate is open for 1024ms 13: Gate is open for 2048ms 14: Gate is open for 4096ms 15: Gate is open for 8192ms 16: Gate is open for 16384ms 17 and all others: Gate is open for 32768ms	0	LPC: r/w
	Select Time base for clock supervision with Period Mode: 0: Period Counter incremented with each master clock 1: Period Counter incremented with each 2nd master clock 2: Period Counter incremented with each 4th master clock 3: Period Counter incremented with each 8h master clock 4: Period Counter incremented with each 16th master clock 5: Period Counter incremented with each 32th master clock 6: Period Counter incremented with each 64th master clock 7: Period Counter incremented with each 128th master clock 8: Period Counter incremented with each 256th master clock 9 and all others: Period Counter incremented with each 512th master clock		
6:5	Reserved	0	r
7	Measurement Mode: 0: Gate Mode. Count positive clock edges during open gate. 1: Period Mode. Count number of clocks which fit in one period.	0	LPC: r/w

Table 5-96 Telecom Clock Monitor Frequency/Period Register

Address: 0x65-0x66			
Bit	**Description**	**Default**	**Access**
15:0	Result of supervised Telecom Clock. Gate mode: 0: No clock edge sampled. Clock to slow for time base 1 - 65534: Number of sampled clocks during timer base. 65535: Overflow. Clock to fast for time base. Period Mode 0: No clock edge sampled. Clock to fast for time base 1 - 65534: Number of clocks during one supervised clock period. 65535: Overflow. Supervised clock to slow for time base. Note: Only valid when corresponding bit in *Table 5-92* Telecom Clock Monitor Status Register is set.	0	LPC: r

Table 5-97 Telecom Clock Monitor Lower Limit Register

Address: 0x67 -0x68			
Bit	**Description**	**Default**	**Access**
15:0	Lower Limit for supervised Telecom Clock: Used by *Table 5-93* Telecom Clock Monitor Out of Range Register.	0	LPC: r/w

Table 5-98 Telecom Clock Monitor Upper Limit Register

Address: 0x69 -0x6A			
Bit	**Description**	**Default**	**Access**
15:0	Upper Limit for supervised Telecom Clock: Used by *Table 5-93*Telecom Clock Monitor Out of Range Register	0xFFFF	LPC: r/w

5.1.28 BIOS Version Registers

Table 5-99 BIOS Version Register 1

Address Offset: 0x74			
Bit	**Description**	**Default**	**Access**
7:0	BIOS Version bits 0 to 7	0	LPC: r/w IPMC: r

Table 5-100 BIOS Version Register 2

Address Offset: 0x75			
Bit	**Description**	**Default**	**Access**
7:0	BIOS Version bits 8 to 15	0	LPC: r/w IPMC: r

Table 5-101 BIOS Version Register 3

Address Offset: 0x76			
Bit	**Description**	**Default**	**Access**
7:0	BIOS Version bits 16 to 23	0	LPC: r/w IPMC: r

5.1.29 IPMC BIOS Communication Registers

Table 5-102 IPMC BIOS Communication Register 1

Address Offset: 0x7A			
Bit	**Description**	**Default**	**Access**
7:0	IPMC BIOS Communication bits	PWR_GOOD: 0	LPC: r/w IPMC: r/w

Table 5-103 IPMC BIOS Communication Register 2

Address Offset: 0x7B			
Bit	**Description**	**Default**	**Access**
7:0	IPMC BIOS Communication bits	PWR_GOOD: 0	LPC: r/w IPMC: r/w

Table 5-104 IPMC BIOS Communication Register 3

Address Offset: 0x7C			
Bit	**Description**	**Default**	**Access**
7:0	IPMC BIOS Communication bits	PWR_GOOD: 0	LPC: r/w IPMC: r/w

5.1.30 Scratch Registers

Table 5-105 LPC Scratch Register

Address Offset: 0x7D			
Bit	**Description**	**Default**	**Access**
7:0	LPC Scratch bits	PWR_GOOD:0	LPC: r/w IPMC: r

Table 5-106 IPMC Scratch Register

Address Offset: 0x7E			
Bit	**Description**	**Default**	**Access**
7:0	LPC Scratch bits	PWR_GOOD:0	IPMC: r/w LPC: r

BIOS

6.1 Introduction

The Basic Input/Output System (BIOS) provides an interface between the operating system and the hardware of the blade. It is used for hardware configuration. Before loading the operating system, BIOS performs basic hardware tests and prepares the blade for the initial boot-up procedure.

During blade production, identical BIOS images are programmed into both boot flash banks. It is possible to select boot flash as device to boot from. This is done via an IPMI command. For further details refer to section *System Boot Options Parameter #96 on page 236*.

The BIOS used on the blade is based on the Insyde UEFI BIOS with several Penguin Edge extensions integrated. Its main features are:

- Initialize CPU, chipset and memory
- Initialize PCI devices
- Setup utility for setting configuration data
- IPMC support
- Serial console redirection for remote blade access
- Boot operation system

The BIOS complies with the following specifications:

- UEFI Specification 2.3.1
- Plug and Play BIOS Specification 1.0a
- PCI BIOS Specification 2.1
- SMBIOS Specification 2.8
- BIOS Boot Specification 1.01
- PXE 2.1
- Multiprocessor Specification 1.4
- ACPI 5.0

The BIOS setup program is required to configure the blade hardware. This configuration is necessary for operating the blade and connected peripherals. The configuration data are stored in the same flash device from which the board boots.

When you are not sure about configuration settings, restore the default values. This option is provided in case a value has been changed and you want to reset settings.

Loading the BIOS default values affect all setup items and reset options previously altered.

If you set the default values, the displayed default values take effect only after the BIOS setup is saved and closed.

6.2 Accessing the Blade Using the Serial Console Redirection

The blade's firmware provides a serial console redirection feature allowing remote access to the blade through a terminal connected to the blade's serial interface.

The terminal can be connected to display VGA text information. Terminal keyboard input is redirected and treated as a normal PC keyboard input. The serial console redirection feature can be configured via a setup utility.

6.2.1 Requirements for Serial Console Redirection

For serial console redirection, the following are required:

- Terminal or terminal emulation which supports a VT100 mode
- NULL-modem cable

Terminal emulation programs such as TeraTermPro or Putty can be used.

6.2.2 Default Access Parameters

By default, the blade can be accessed using the serial interface COM1. By default, this interface is accessible using an RJ-45 connector at the blade's face plate.

A NULL-Modem cable is available as accessory kit for the blade. It converts the RJ-45 connector to a standard DSUB connector which can be connected to a remote terminal. By default, The following communication parameters are used:

- Baud rate: 115200
- Flow control: None
- VT-100
- Eight data bits
- No parity
- One stop bit

6.2.3 Connecting to the Blade

Procedure

To connect to the blade using the serial console redirect feature:

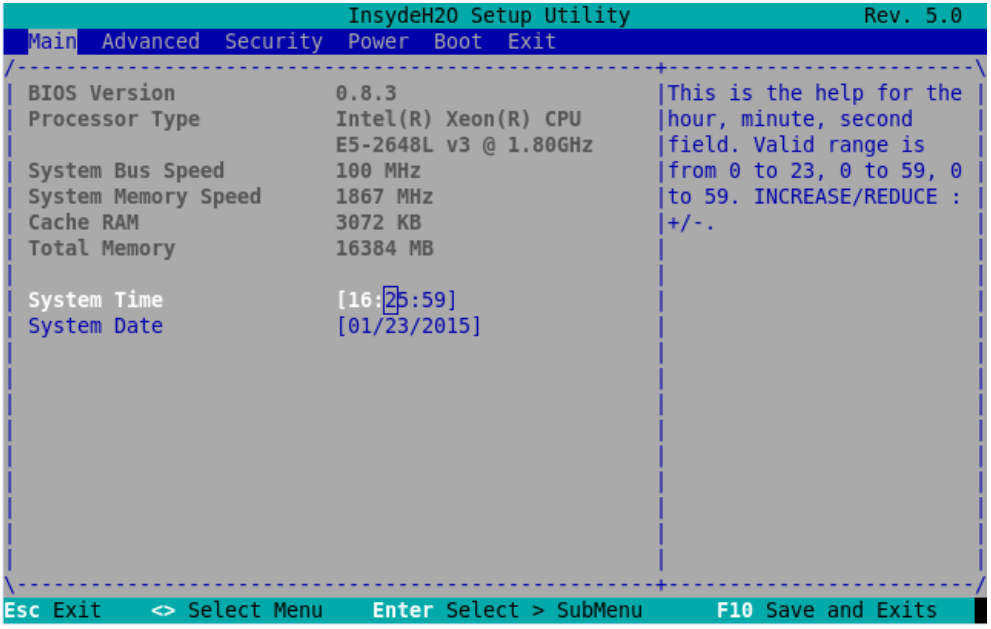
1. Configure terminal to communicate using the same parameters as in BIOS setup.
2. Connect the terminal to NULL-modem cable.
3. Connect the NULL-modem cable to COM port of the blade.
4. Start up the blade.

6.3 Changing Configuration Settings

When the system is switched on or rebooted, the presence and functionality of the system components is tested by Power-On Self-Test (POST).

Press <F2> key when requested. The main menu appears. It looks similar to the one shown in the following figure.

Figure 6-1 Main Menu



Make sure BIOS is properly configured prior to installing the operating system and its drivers.

If you save changes in setup, the next time the blade boots up, BIOS configures the system according to the setup selections stored. If those values cause the system boot to fail, reboot and enter setup to get the default values or to change the selections that caused the failure.

In order to navigate in setup, use the arrow keys on the keyboard to highlight items on the menu. All other navigation possibilities are shown at the bottom of the menu.

Additionally, an item-specific help is displayed on the right side of the window.

6.4 Boot Support

6.4.1 Boot Mode

BIOS supports **UEFI** boot mode and **Legacy** boot mode.

Legacy boot mode refers to BIOS boot mode introduced by IBM on their first Personal Computer. UEFI boot mode is specified in the UEFI specification.

Legacy boot from a hard disk uses the Master Boot Record (MBR) partition scheme, whereas UEFI boot mode uses the GUID Partition Table (GPT).

Legacy boot maintains a list of all devices which may be of bootable type (for example, SATA devices, network devices).

In UEFI boot mode, BIOS maintains a list of operating system loaders, which are present in the so called EFI System Partition. The EFI System Partition is a small partition (~100Mbyte) with FAT32 file system, which contains the OS loader.

During the POST procedure the UEFI BIOS scans all storage devices that are connected to the system for a valid GUID Partition Table (GPT). If there is a known boot loader found in the EFI System Partition, a new entry is added to the boot order list. For example, if the EFI System Partition contains the \EFI\redhat\grub.efi file, BIOS will add Red Hat Linux to the boot list.

In UEFI boot mode, network devices are handled in the same way as in legacy mode, they are simply added to the boot order list.

A detailed description of UEFI boot mechanism can be found in the UEFI Specification chapter 3 Boot Manager and chapter 5 GUID Partition Table (GPT) Disk Layout (*http://www.uefi.org/specifications*).

6.4.2 Boot Type

In BIOS Setup **Boot Menu** the following Boot Type can be selected:

- Dual Boot Type
  Legacy and UEFI Boot is enabled. With the Boot Priority option, you can determine whether UEFI devices or legacy devices are placed first in the boot order list. Additionally with the setup option **PXE Boot capability** the type of network boot can be selected between **legacy** and **UEFI**.

NOTE: If Legacy devices are placed first in the boot order list, the UEFI devices are not executed and the board will be automatically restarted. This is a limitation of the Legacy Compatibility Support Module of the BIOS.

- Legacy Boot Type
  Only legacy boot devices are in the boot order list.
- UEFI Boot Type
  Only UEFI boot devices/OS loader are in the boot order list.

6.4.3 Supported Boot Devices

The BIOS supports booting from the following devices/sources:

- Solid State Disk connected to the SATA interface (available only when SSD SATA is assembled).
- USB devices, floppy, CD ROM, and hard disk.
- PXE boot from Front Panel Ethernet, Base Ethernet and Fabric Ethernet.

6.4.4 Selecting the Boot Device

To determine the device from which BIOS attempts to boot, the following are the possibilities:

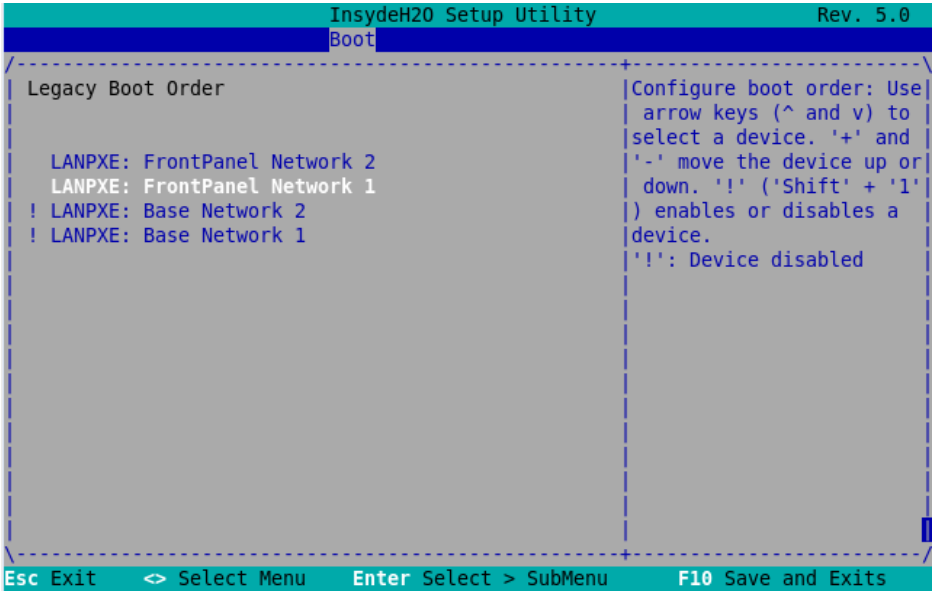
- By setup, to select a permanent order of boot devices
- By boot selection menu, to select any device for the next boot-up procedure only
- By changing the *bootorder* parameter of IPMI Boot parameter. For more information, refer to sections *IPMI Boot Parameter on page 186* and *System Boot Options Parameter #100 on page 237*.

By Setup

To select the boot device by setup, proceed as follows:

1. From the BIOS setup menu, select **Boot**.
2. Select **Legacy Boot Order** and/or **EFI Boot Order**.

Figure 6-2 Boot Device Priority



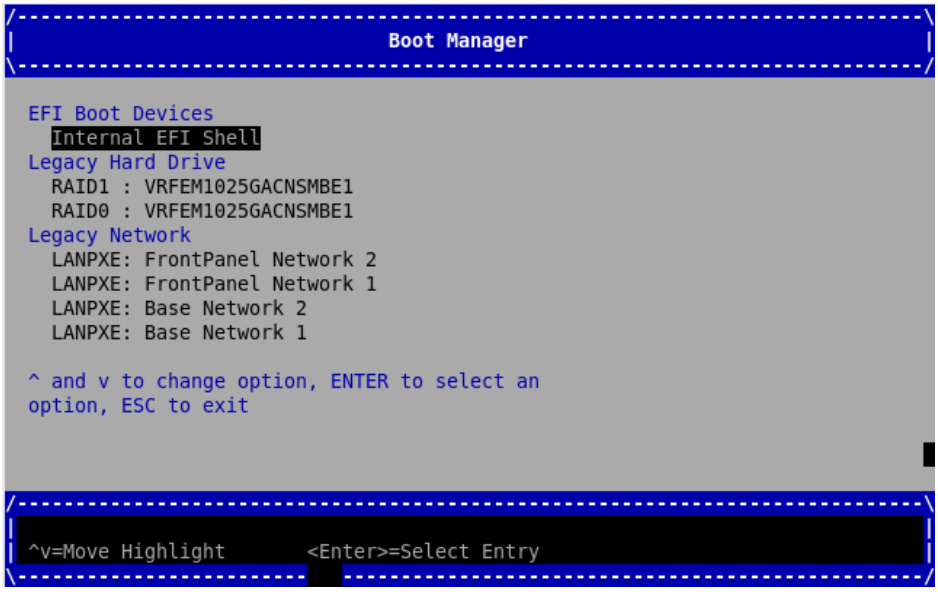
3. Select the order of the devices from which BIOS attempts to boot the operating system.

If BIOS is not successful at booting from one device, it tries to boot from the next device on the list. When BIOS does not find any bootable device, the board will be restarted by a cold reset.

6.4.5 By Boot Menu

1. Press <F4> key to enter the **Boot** menu.
2. Enter **Boot Manager**.

Figure 6-3 Boot Menu



3. Override existing boot sequence by selecting another boot device from the boot list.

If a selected legacy boot device does not load the operating system, BIOS will reset the blade.

If an EFI boot device does not load the operating system, it will return to the Boot Manager.

6.5 iSCSI Boot

BIOS supports iSCSI boot in UEFI mode from Front Panel Ethernet, Base Ethernet and Fabric Ethernet. The following chapter describes the iSCSI configuration menu.

Ensure that in the BIOS Setup, in the Boot Menu the Boot Type is set to Dual Boot Type or UEFI Boot Type, and the PXE Boot capability is set to UEFI:IPv4.

Steps to configure iSCSI boot:

1. Enter the Boot Menu/Front Page by pressing the <F4> key
2. Select Device Manager from the Boot Menu.
3. Select the iSCSI Configuration Menu.
4. Enter an iSCSI Initiator Name.
5. Add one or more iSCSI Attempts.
6. Save the iSCSI configuration with F10 key.

iSCSI Configuration

Figure 6-4 iSCSI Configuration

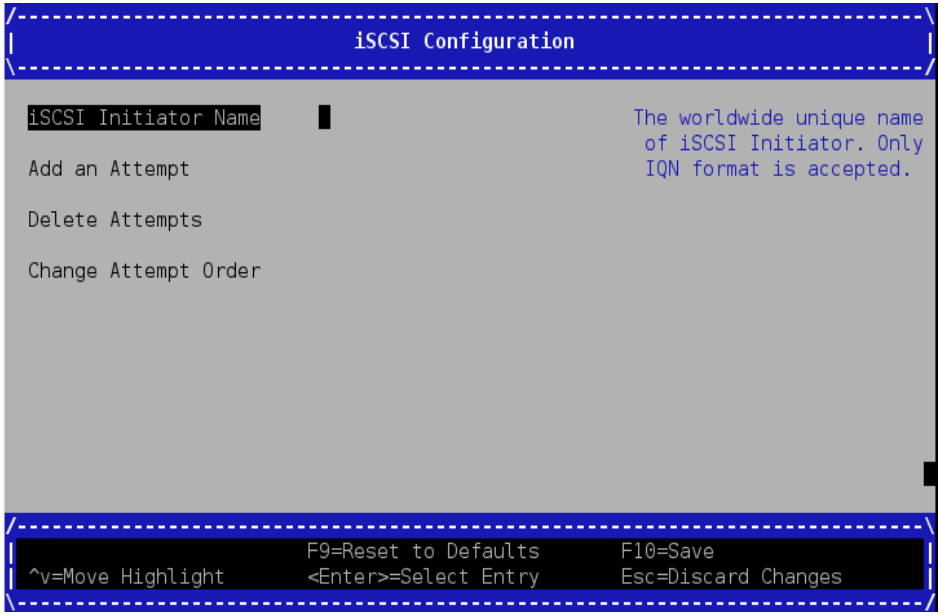


Table 6-1 iSCSI Configuration Menu

Item	Values	IPMI Boot Parameter	Description
ISCSI Initiator Name	--	--	The worldwide unique name of the iSCSI Initiator. Only IQN format is accepted.
Add Attempt			Add an iSCSI Attempt
Delete Attempts			Delete an iSCSI Attempt
Change Attempt Order			Change the order of iSCSI Attempts

Add an ISCSI Attempt

Figure 6-5 Attempt Configuration 1

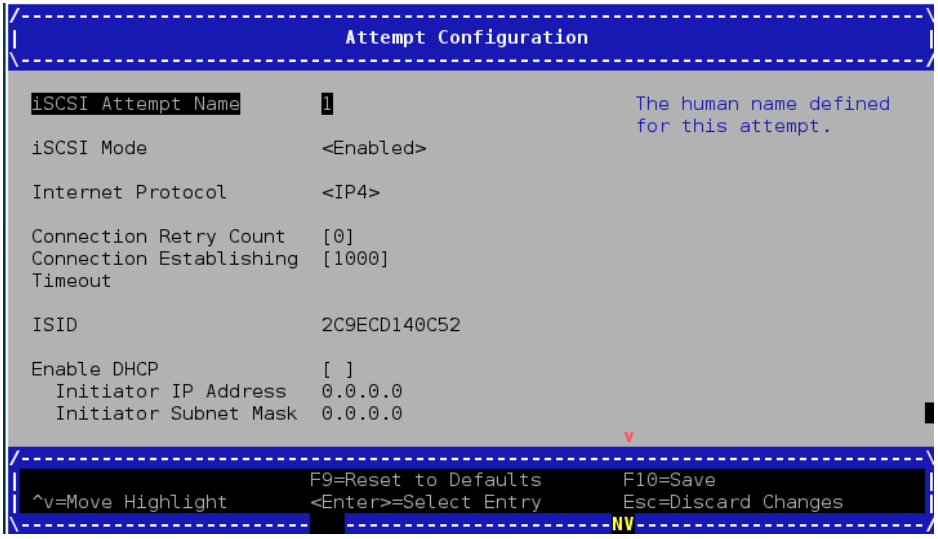


Figure 6-6 Attempt Configuration 2

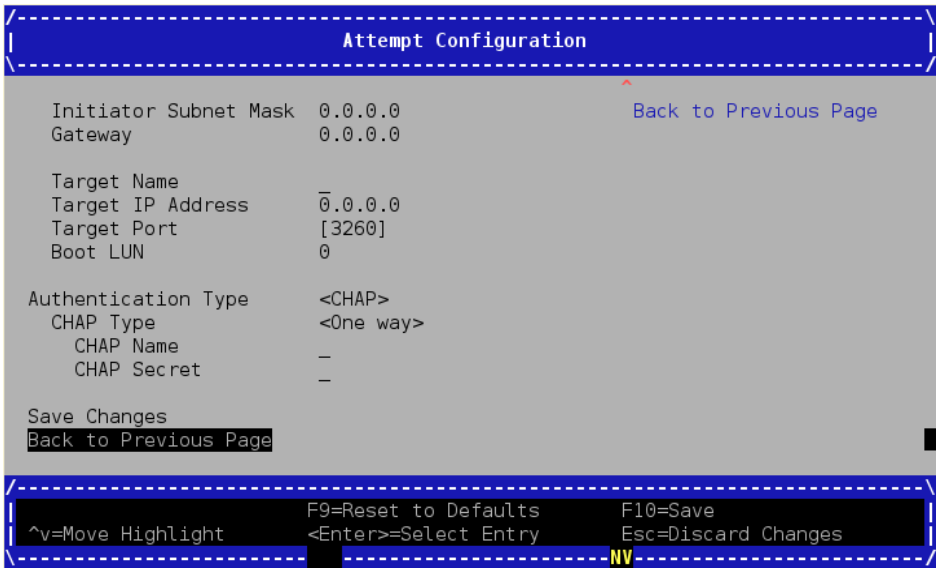


Table 6-2 Add an iSCSI Attempt Menu

Item	Values	IPMI Boot Parameter	Description
iSCSI Mode	Disabled/Enabled/Enabled for MPIO	--	Set to Enabled. Use Enabled for MPIO (Multipath I/O if your target is also configured for Multipath I/O. MPIO
Internet Protocol	IP4/IP6/Autoconfigure		Can be set to IP4, IP6, or Autoconfigure. In Autoconfigure mode, the iSCSI driver attempts to connect to the iSCSI target using the IPv4 stack. If this fails, then the iSCSI driver attempts to connect using the IPv6 stack.
Connection Retry Count The count range is 0 to 16. If set to 0, there are no retries.	0..40		The minimum value is 0 and the maximum is 40. 0 means no retry. It will stall 1 second and reconnect.

Table 6-2 Add an iSCSI Attempt Menu (continued)

Item	Values	IPMI Boot Parameter	Description
Connection Establishing Timeout	100 … 20000		The timeout value in milliseconds. The minimum value is 100 milliseconds and the maximum is 20 seconds.
Configure ISID	Derived from the MAC address		The OUI-format ISID is 6 bytes. The default value is derived from the MAC address. Only the last 3 bytes are configurable. Example: Update 0ABBCCDDEEFF to 0ABBCCF07901 by inputting F07901
Enable DHCP	Disabled/Enabled		Enable or disable DHCP
Initiator IP Address	--		Use to set initiator IP address in dotted-decimal notation.
Initiator Subnet Mask	--		Use to set initiator subnet mask IP address in dotted-decimal notation.
Gateway	--		Use to set initiator gateway IP address in dotted-decimal notation.
Target Name	--		The worldwide unique name of the target. Only IQN format is accepted.
Target IP address	--		Use to set target IP address in dotted-decimal notation.
Target Port	--		Use to change target port number. Default is 3260.
Boot LUN	--		Use to set the hexadecimal representation of the boot logical unit number (LUN). Example: 4752-3A4F-6b7e-2F99
Authentication Type	CHAP/None		Define the Challenge-Handshake Authentication Protocol (CHAP). Available settings are CHAP, Kerberos, and None.

Table 6-2 Add an iSCSI Attempt Menu (continued)

Item	Values	IPMI Boot Parameter	Description
CHAP Type	One Way/Mutual		Use to set CHAP type to either One Way or Mutual.
CHAP Name	--		Set the CHAP name.
CHAP Secret	--		Use to set the CHAP secret password. The secret length range is 12 to 16 bytes.
Save Changes	--		Save Changes. The system must be rebooted manually for changes to take place.
Back to Previous Page	--		Back to Previous Page

6.6 IPMI Boot Parameter

Many BIOS setup parameters and setup default parameters are stored as Intelligent Platform Management Interface (IPMI) boot parameters within a non-volatile memory controlled by the Intelligent Platform Management Controller (IPMC). IPMI boot parameter supports USER and DEFAULT area. The USER area contains the current BIOS setup settings. The parameters in the USER area can be modified by the BIOS setup utility and can also be modified remotely by IPMI commands. For example, through shelf manager.

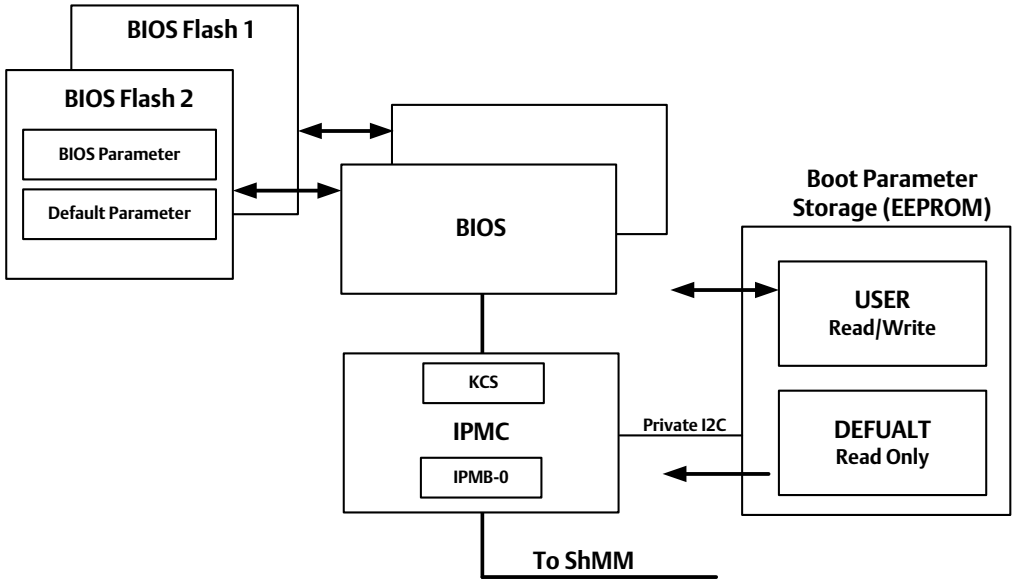
The DEFAULT area holds the BIOS default settings. This area is read only. BIOS default settings are loaded when selecting the Restore Defaults Item on BIOS Save and Exit Menu.

A detailed description of the IPMI Boot Parameter and the corresponding IPMI commands is available in *System Boot Options Parameter #100 on page 237*.

The main advantage of using IPMI boot parameter is that the parameters stored as IPMI boot parameters are not changed after a BIOS upgrade or a BIOS boot bank switch. BIOS will not return to the BIOS default settings after a BIOS upgrade.

Normally, the BIOS setup parameters are stored within the BIOS flash. The following figure and description helps you to understand how a BIOS setup parameter and an IPMI boot parameter interact.

Figure 6-7 IPMI Boot Parameter



Board Start

1. BIOS loads BIOS Parameter from Flash and uses them for initialization.
2. BIOS loads IPMI Boot Parameter from USER area.
3. BIOS updates the BIOS Parameter in the flash according to the IPMI Boot Parameter.
4. BIOS will reset the board if BIOS Parameter changes.

Change Settings

1. User enters the BIOS setup and changes some parameters.
2. User selects **Save** or **Save and Exit option**.
3. BIOS writes the parameter to the BIOS Parameter in the Flash.
4. BIOS writes the parameter to the IPMI Boot Parameter USER area.

Load Defaults

1. User enters BIOS setup and selects Load Defaults.

2. BIOS reads Default Parameter from Flash into the Setup.
3. BIOS reads IPMI Boot Parameter DEFAULT area into the Setup.
4. User selects **Save** or **Save and Exit option**.
5. BIOS writes the parameter to the BIOS Parameter in the Flash.
6. BIOS writes the parameter to the IPMI Boot Parameter USER area.

6.7 BIOS Setup Configuration

This section provides information about the various configurations at BIOS setup.

6.7.1 Main

The following figure shows the Main menu options.

Figure 6-8 Main Menu Options

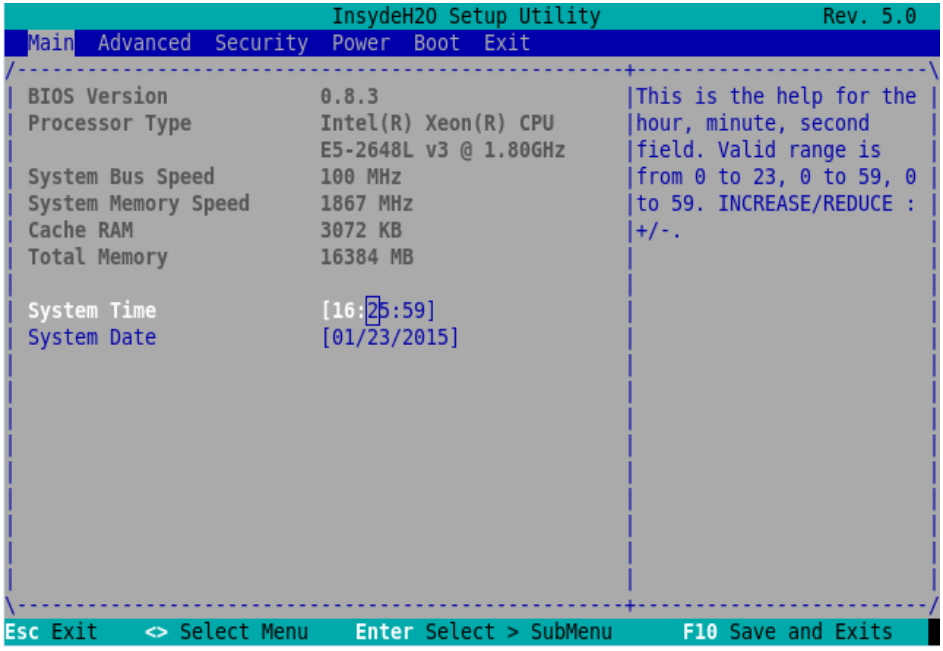


Table 6-3 Main Menu

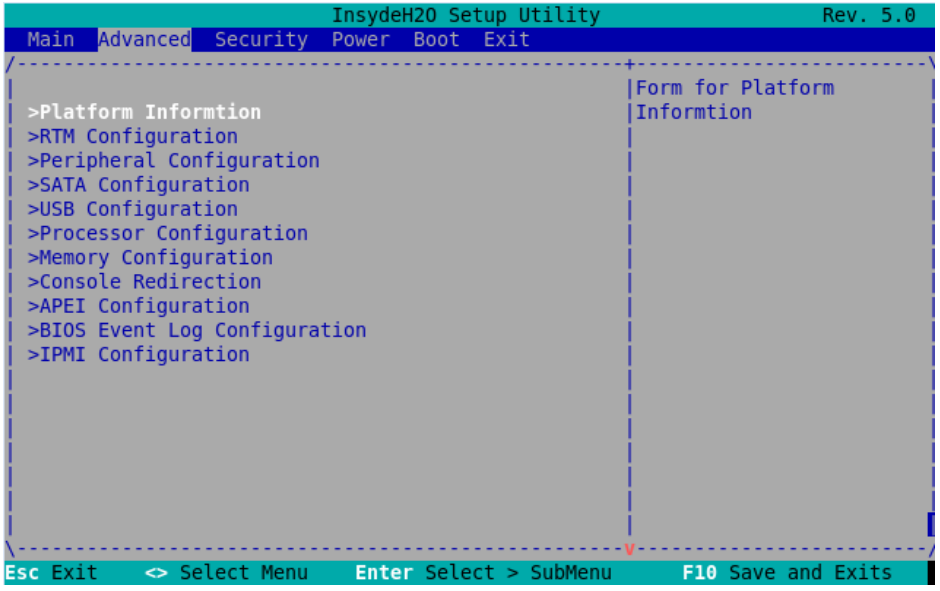
Item	Values	IPMI Boot Parameter	Description
System Time	[15:48:21]	--	Set the Time. Use Enter to switch between Time elements.
System Date	[Thu 11/11/2014]	--	Set the Date. Use Enter to switch between Date elements.

6.7.2 Advanced

Platform Information

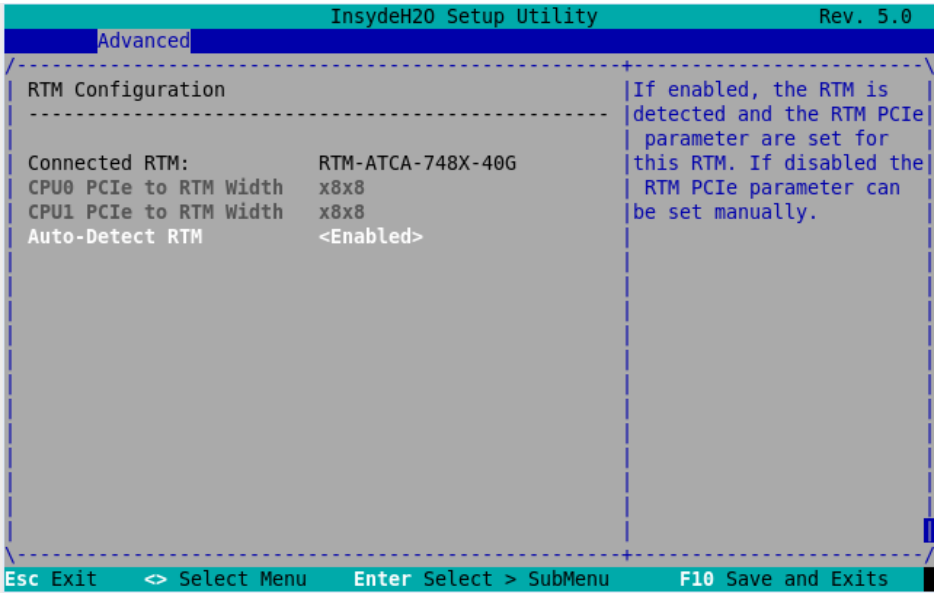
This option shows important information about Platform, CPU, QPI, and Memory.

Figure 6-9 Platform Information



RTM Configuration

Figure 6-10 RTM Configuration



The following table contains description about the options that can be configured in RTM configuration.

Table 6-4 Advanced >> RTM Configuration

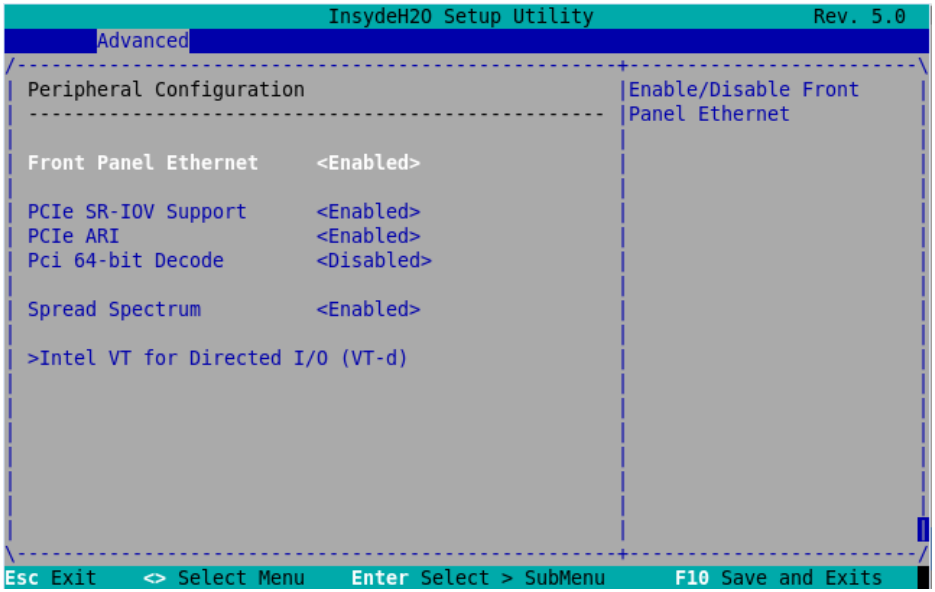
Item	Values	IPMI Boot parameter	Description
Auto-Detect RTM	Enabled, Disabled	rtm_auto	If enabled, the RTM is detected and the RTM PCI Express parameter are set for this RTM. If disabled, the RTM PCI Express parameter can be set manually.
CPU0 PCIe to RTM Width	X4x4x4x4 x4x4x8 x8x4x4 x8x8	rtm_cpu0_bif	SelectsCPU0PCIeBifurcationforZone3 connector (RTM)
CPU0 PCIe Port 3A	Auto Gen 1 (2.5 GT/s) Gen 2 (5 GT/s) Gen 3 (8 GT/s)	rtm_cpu0_3a	Selects CPU0 PCIe Port 3A Speed for Zone 3 connector (RTM)

Table 6-4 Advanced >> RTM Configuration (continued)

Item	Values	IPMI Boot parameter	Description
CPU0 PCIe Port 3B	Auto Gen 1 (2.5 GT/s) Gen 2 (5 GT/s) Gen 3 (8 GT/s)	rtm_cpu0_3b	Selects CPU0 PCIe Port 3B Speed for Zone 3 connector (RTM)
CPU0 PCIe Port 3C	Auto Gen 1 (2.5 GT/s) Gen 2 (5 GT/s) Gen 3 (8 GT/s)	rtm_cpu0_3c	Selects CPU0 PCIe Port 3C Speed for Zone 3 connector (RTM)
CPU0 PCIe Port 3D	Auto Gen 1 (2.5 GT/s) Gen 2 (5 GT/s) Gen 3 (8 GT/s)	rtm_cpu0_3d	Selects CPU0 PCIe Port 3D Speed for Zone 3 connector (RTM)
CPU1 PCIe to RTM Width	X4x4x4x4 x4x4x8 x8x4x4 x8x8	rtm_cpu1_bif	Selects CPU1 PCIe Bifurcation for Zone 3 connector (RTM)
CPU1 PCIe Port 3A	Auto Gen 1 (2.5 GT/s) Gen 2 (5 GT/s) Gen 3 (8 GT/s)	rtm_cpu1_3a	Selects CPU1 PCIe Port 3A Speed for Zone 3 connector (RTM)
CPU1 PCIe Port 3B	Auto Gen 1 (2.5 GT/s) Gen 2 (5 GT/s) Gen 3 (8 GT/s)	rtm_cpu1_3b	Selects CPU1 PCIe Port 3B Speed for Zone 3 connector (RTM)
CPU1 PCIe Port 3C	Auto Gen 1 (2.5 GT/s) Gen 2 (5 GT/s) Gen 3 (8 GT/s)	rtm_cpu1_3c	Selects CPU1 PCIe Port 3C Speed for Zone 3 connector (RTM)
CPU1 PCIe Port 3D	Auto Gen 1 (2.5 GT/s) Gen 2 (5 GT/s) Gen 3 (8 GT/s)	rtm_cpu1_3d	Selects CPU1 PCIe Port 3D Speed for Zone 3 connector (RTM)

Peripheral Configuration

Figure 6-11 Peripheral Configuration



The following table contains description about the options that can be configured in Peripheral configuration.

Table 6-5 Advanced >> Peripheral Configuration

Item	Values	IPMI Boot parameter	Description
Front Panel Ethernet	Enabled, Disabled	frontnet	Enables/Disables Front Panel Ethernet
PCIe SR-IOV Support	Enabled, Disabled	pci_sriov	Enables/Disables PCI Express Single Root I/O Virtualization
PCIe ARI	Enabled, Disabled	pci_ari	Enables/Disables Alternative Routing ID Interpretation (ARI)
Pci 64-bit Decode	Enabled, Disabled	pci_64bit	Allows system to support 64-bit BAR for PCI devices
Spread Spectrum	Enabled, Disabled	clock_ssc	Enables/Disables Spread Spectrum Clock setting to affect EMI Front Panel Ethernet

Figure 6-12 Peripheral Intel VT Configuration

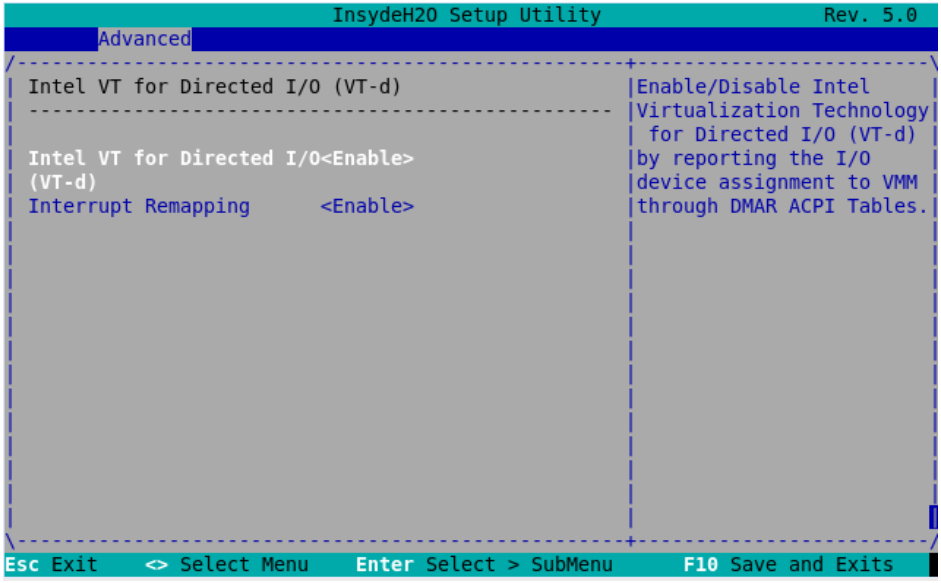
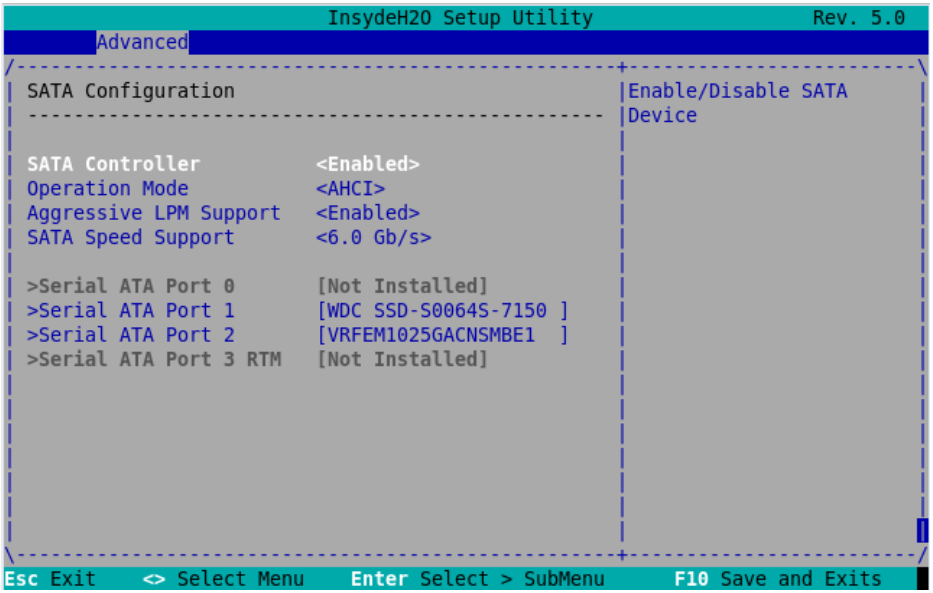


Table 6-6 Advanced >> Peripheral Configuration >> Intel VT for Directed I/O (VT-d)

Item	Values	IPMI Boot Parameter	Description
Intel VT for Directed I/O (VT-d)	Enabled, Disabled	vtd	Enables/Disables Intel Virtualization Technology for Directed I/O (VT-d) by reporting the I/O device assignment to VMM through DMAR ACPI Tables
Interrupt Remapping	Enabled, Disabled	vtd_ir	Enables/Disables VT_D Interrupt Remapping Support

SATA Configuration

Figure 6-13 SATA Configuration



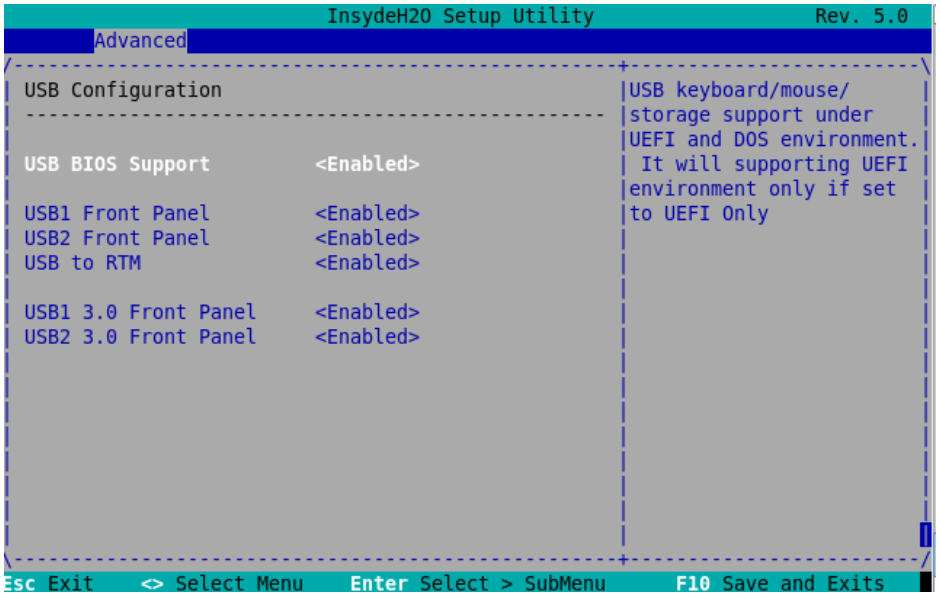
The following table contains description about the options that can be configured in SATA configuration.

Table 6-7 Advanced >> SATA Configuration

Item	Values	IPMI Boot Parameter	Description
SATA Controller	Enabled, Disabled	sata	Enables/Disables SATA Device
Operation Mode	IDE, AHCI, RAID	sata_mode	Selects the controllers Operation Mode
RAID OROM prompt delay	2, 4, 6, 8 Seconds	sata_raidwait	Time for delay of SATA RAID Option ROM prompt
Aggressive LPM Support	Enabled, Disabled	sata_alpm	Enables/Disables Aggressive Link Power Management (SALP)
SATA Speed Support	1.5 Gb/s, 3.0 Gb/s, 6.0 Gb/s	sata_speed	Indicates the maximum speed the SATA controller can support on its ports (Only usable in AHCI/RAID mode)

USB Configuration

Figure 6-14 USB Configuration



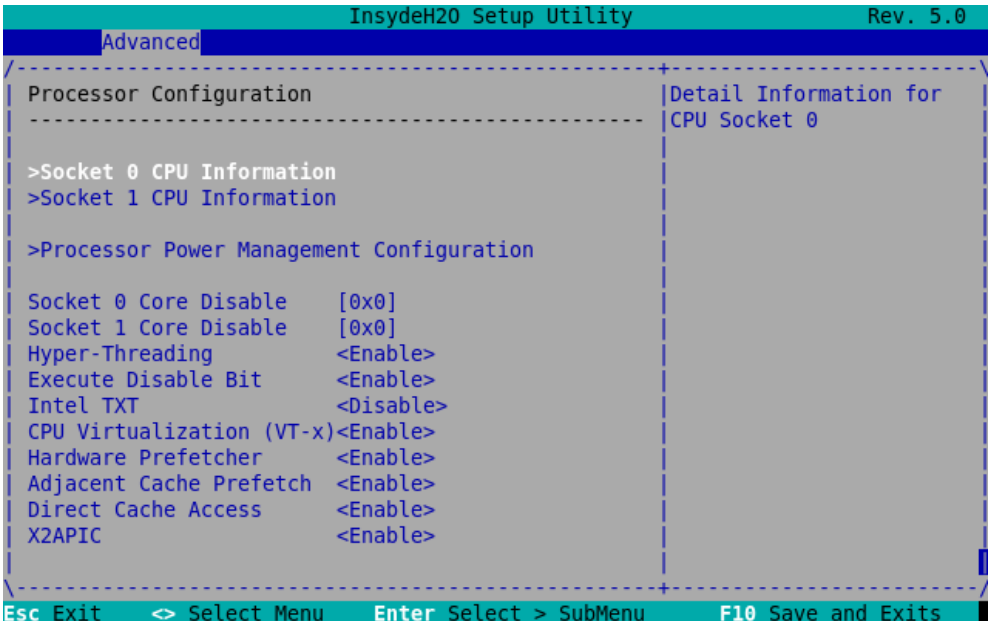
The following table contains description about the options that can be configured in USB configuration.

Table 6-8 Advanced >> USB Configuration

Item	Values	IPMI Boot Parameter	Description
USB BIOS Support	Enabled, Disabled, UEFI Only	usb	Enables/Disables USB keyboard/mouse/storage support under UEFI and DOS environment. If UEFI Only is set, it supports only in UEFI environment.
USB1 Front Panel	Enabled, Disabled	usb1	Enables/Disables USB Front Panel Port 1
USB2 Front Panel	Enabled, Disabled	usb2	Enables/Disables USB Front Panel Port 2
USB to RTM	Enabled, Disabled	usb_rtm	Enables/Disables USB to RTM
USB1 3.0 Front Panel	Enabled, Disabled	usb1_3	Enables/Disables USB1 Front Panel USB 3.0 support
USB2 3.0 Front Panel	Enabled, Disabled	usb2_3	Enables/Disables USB2 Front Panel USB 3.0 support

CPU Configuration

Figure 6-15 CPU Configuration



The following table contains description about the options that can be configured in CPU configuration.

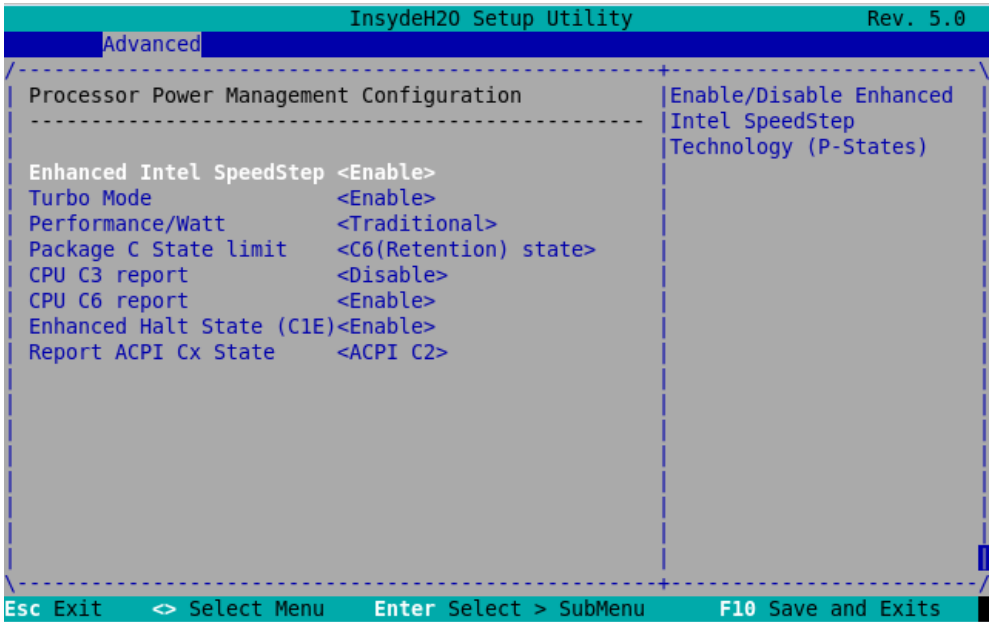
Table 6-9 Advanced >> Processor Configuration

Item	Values	IPMI Boot Parameter	Description
Socket 0 Core Disable	0 to 3FFE	cpu0_dism	Core Disable Bitmap Hex Value 0: Enable all cores Valid Range: 0 to 3FFE 3FFF=Disabling all cores: Invalid
Socket 1 Core Disable	0 to 3FFE	cpu1_dism	Core Disable Bitmap Hex Value 0: Enable all cores Valid Range: 0 to 3FFE 3FFF=Disabling all cores: Invalid
Hyper-Threading	Enabled, Disabled	cpu_ht	Enables Hyper Threading Software Method to Enable/Disable Logical Processor threads
Execute Disable Bit	Enabled, Disabled	cpu_ed	When disabled, forces the XD feature flag to always return 0

Table 6-9 Advanced >> Processor Configuration (continued)

Item	Values	IPMI Boot Parameter	Description
Intel TXT	Enabled, Disabled	cpu_txt	Enables/Disables the Intel Trusted Execution Technology (TXT)
CPU Virtualization (VT-x)	Enabled, Disabled	cpu_vt	Enables processor hardware support to improve the virtualization performance and robustness
Hardware Prefetcher	Enabled, Disabled	cpu_hp	Enables/ Disables the hardware prefetcher.
Adjacent Cache Prefetch	Enabled, Disabled	cpu_acp	When enabled, optimizes the system for applications that require high utilization of sequential memory access. When disabled, optimizes the system for applications that require high utilization of random memory access.
Direct Cache Access	Enabled, Disabled	cpu_dca	Enables/Disables Direct Cache Access (DCA)
X2APIC	Enabled, Disabled	cpu_x2apic	Enables/Disables extended APIC support

Figure 6-16 Processor Power Management Configuration



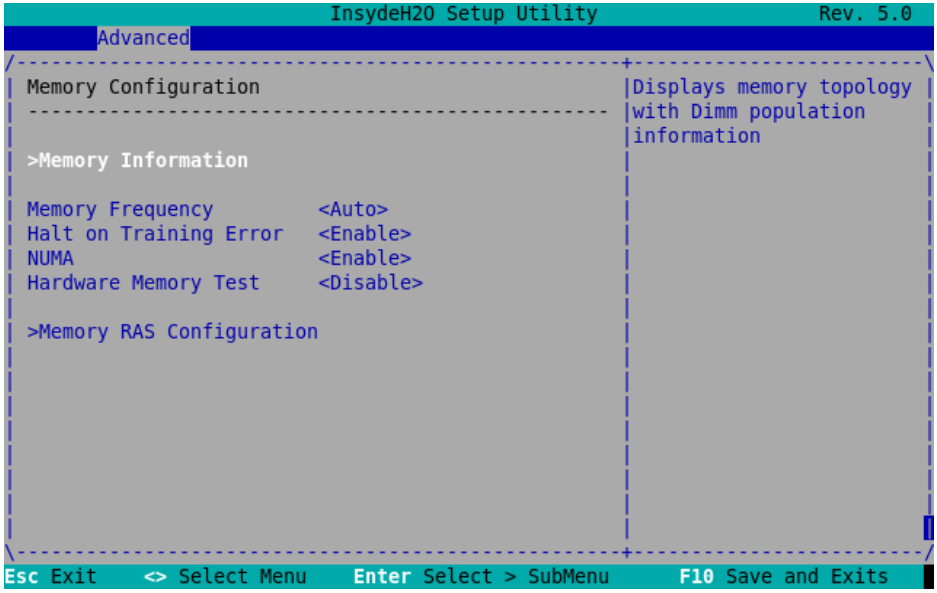
The following table contains description about the options that can be configured in Processor Power Management configuration.

Table 6-10 Advanced >> Processor Configuration >> Processor Power Management Configuration

Item	Values	IPMI Boot Parameter	Description
Enhanced Intel SpeedStep	Enabled, Disabled	cpu_ss	Enables/Disables Enhanced Intel SpeedStep Technology (P-States)
Turbo Mode	Enabled, Disabled	cpu_tm	Enables/Disables processor Turbo Mode
Performance/ Watt	Traditional, Power Optimized	cpu_ppw	When Power Optimized is selected, Intel Turbo Boost Technology engages after performance state P0 is sustained for more than 2 seconds. When Traditional is selected, Intel Turbo Boost Technology is engaged even for P0 requests less than 2 seconds.
CPU C-State	Enabled, Disabled	cpu_cstates	Enables processor idle power saving states (C-States)
Package C State limit	C0/C1 state, C2 state, C6 (non Retention) state, C6 (Retention) state, No Limit	cpu_cslimit	Specifies the lowest C-state for the package. Higher C States will save more power, Lower C States will have lower wake up latencies.
CPU C3 report	Enabled, Disabled	cpu_c3	Enables/Disables CPU C3 (ACPI C3) report to OS
CPU C6 report	Enabled, Disabled	cpu_c6	Enables/Disables CPU C6 (ACPI C3) report to OS
Enhanced Halt State (C1E)	Enabled, Disabled	cpu_c1e	Enables the Enhanced C1E state of the CPU
Report ACPI Cx State	ACPI C2, ACPI C3	cpu_cxacpi	Report CPU C3/C6 state to OS as ACPI C2 or ACPI C3 state

Memory Configuration

Figure 6-17 Memory Configuration

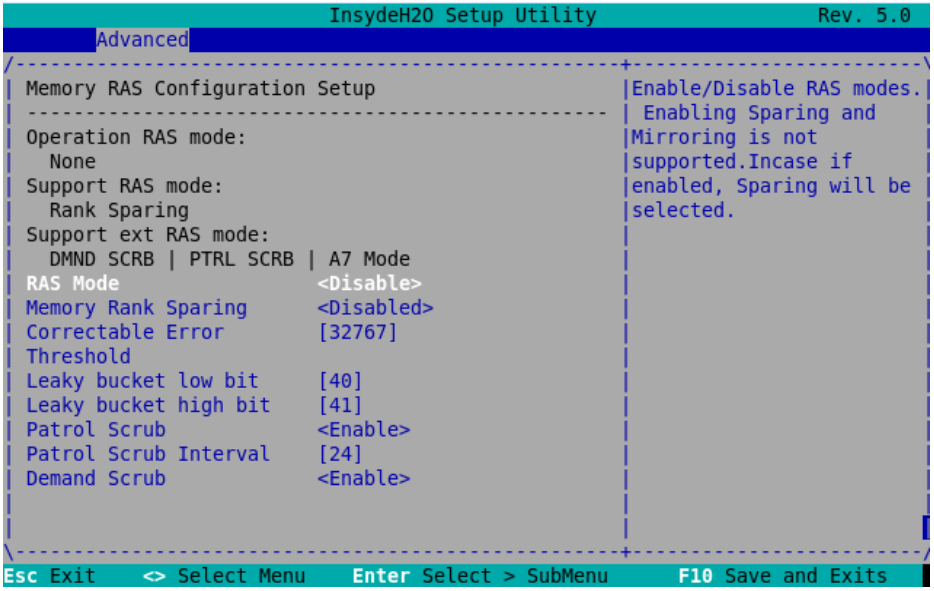


The following table contains description about the options that can be configured in Memory configuration.

Table 6-11 Advanced >> Memory Configuration

Item	Values	IPMI Boot Parameter	Description
Memory Frequency	Auto, 1333, 1600, 1867, 2133	mem_speed	Maximum Memory Frequency Selections in MHz
Halt on Training Error	Enabled, Disabled	mem_halt	Enables/Disables Halt on Memory Training Error
NUMA	Enabled, Disabled	mem_numa	Enables/Disables Non Uniform Memory Access (NUMA)
Hardware Memory Test	Disabled, Short, Long	mem_test	Select Hardware Memory Test

Figure 6-18 Memory RAS Configuration



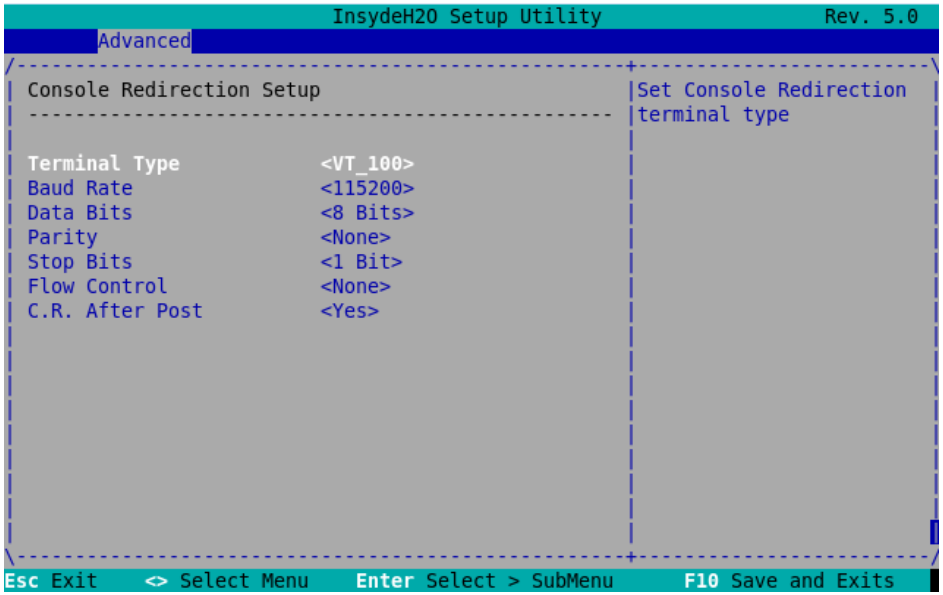
The following table contains description about the options that can be configured in Memory RAS configuration.

Table 6-12 Advanced >> Memory Configuration >> Memory RAS Configuration

Item	Values	IPMI Boot Parameter	Description
RAS Mode	Disable, Mirror, Lockstep Mode	mem_ras	Enables/Disables RAS modes. Enabling Sparing and Mirroring is not supported. In case if enabled, Sparing will be selected.
Memory Rank Sparing	Enabled, Disabled	mem_sparing	Enables/Disables Memory Rank Sparing
Patrol Scrub	Enabled, Disabled	mem_ps	Enables/Disables Patrol Scrub
Demand Scrub	Enabled, Disabled	mem_ds	Enables/Disables Demand Scrub

Console Redirection

Figure 6-19 Console Redirection



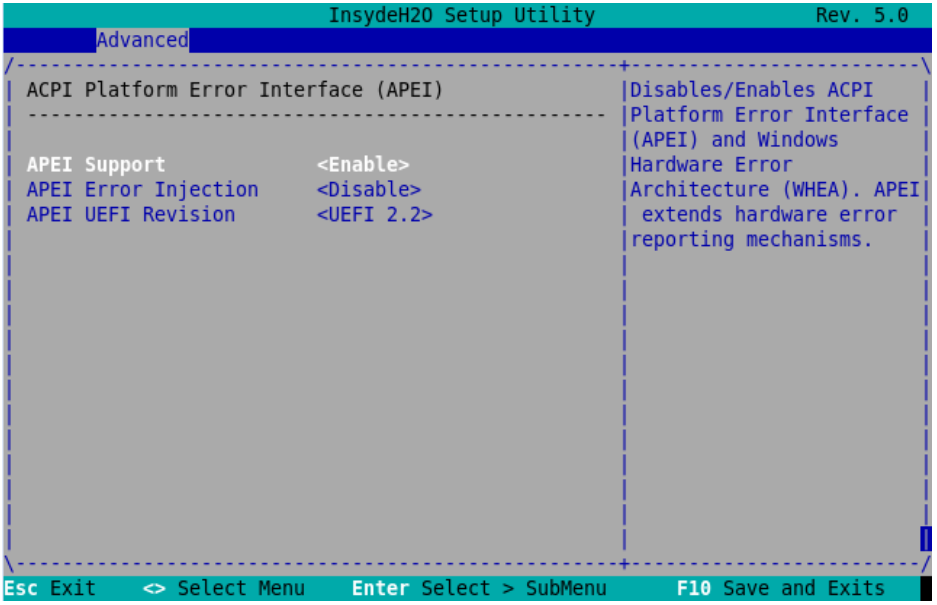
The following table contains description about the options that can be configured for Console Redirection.

Table 6-13 Advanced >> Console Redirection

Item	Values	IPMI Boot Parameter	Description
Terminal Type	VT_100, VT_100+, VT_UTF8, PC_ANSI	con_tt	Sets Console Redirection terminal type
Baud Rate	115200, 57600, 38400, 19200, 9600, 4800, 2400, 1200	con_br	Sets Console Redirection baud rate
Data Bits	7 Bits, 8 Bits	con_db	Sets Console Redirection data bits
Parity	None, Even, Odd	con_par	Sets Console Redirection parity bits
Stop Bits	1 Bit, 2 Bits	con_sb	Sets Console Redirection stop bits
Flow Control	None, XON/XOFF	con_fc	Sets Console Redirection flow control type
C.R. After Post	Yes, No	con_ap	Continue Console Redirection after POST, when OS is loaded

APEI Configuration

Figure 6-20 APEI Configuration



The following table contains description about the options that can be configured in APEI configuration.

Table 6-14 Advanced >> APEI Configuration

Item	Values	IPMI Boot Parameter	Description
APEI Support	Enabled, Disabled	apei	Disables/Enables ACPI Platform Error Interface (APEI) and Windows Hardware Error Architecture (WHEA). AEPI extends hardware error reporting mechanisms and brings them together as components of a coherent hardware error infrastructure.
APEI Error Injection	Disabled, MEMORY_CE, MEMORY_UE_NON_FATAL, MEMORY_UE_FATAL, PCIE_CE, PCIE_UE_NON_FATAL, PCIE_UE_FATAL	--	Inject an error to test APEI feature

Table 6-14 Advanced >> APEI Configuration (continued)

Item	Values	IPMI Boot Parameter	Description
APEI UEFI Revision	UEFI 2.2, UEFI 2.3.1	apei_uefiver	UEFI revision of APEI error format

Table 6-15 Advanced >> BIOS Event Log Configuration

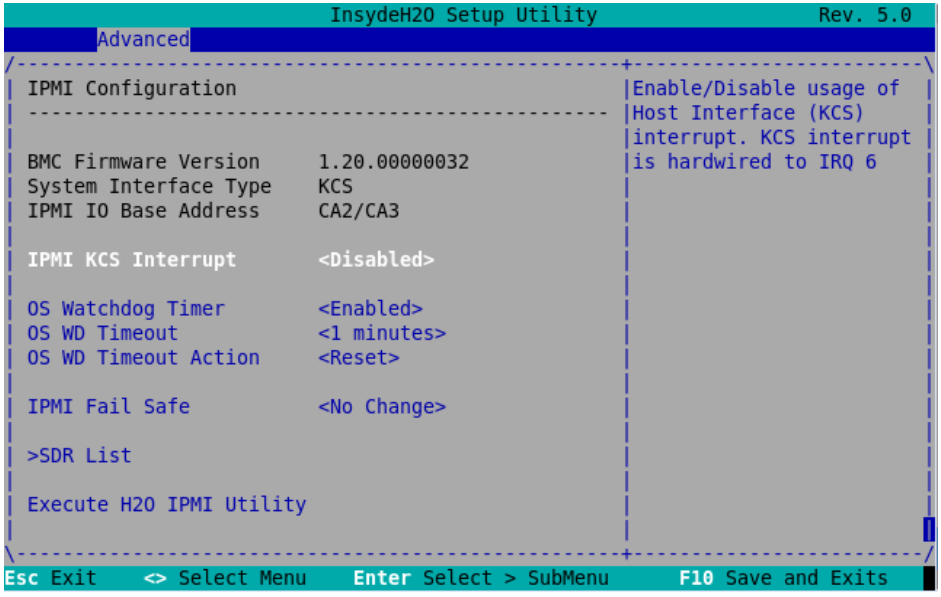
Item	Values	IPMI Boot Parameter	Description
Log Event To	ALL, BIOS, BMC SEL, MEMORY	--	Settings Events to log Selected Storage

Advanced >> BIOS Event Log Configuration >> Event Log Viewer

The Event Log Viewer is used to view the event logs of all storages.

IPMI Configuration

Figure 6-21 IPMI Configuration



The following table contains description about the options that can be configured in IPMI configuration.

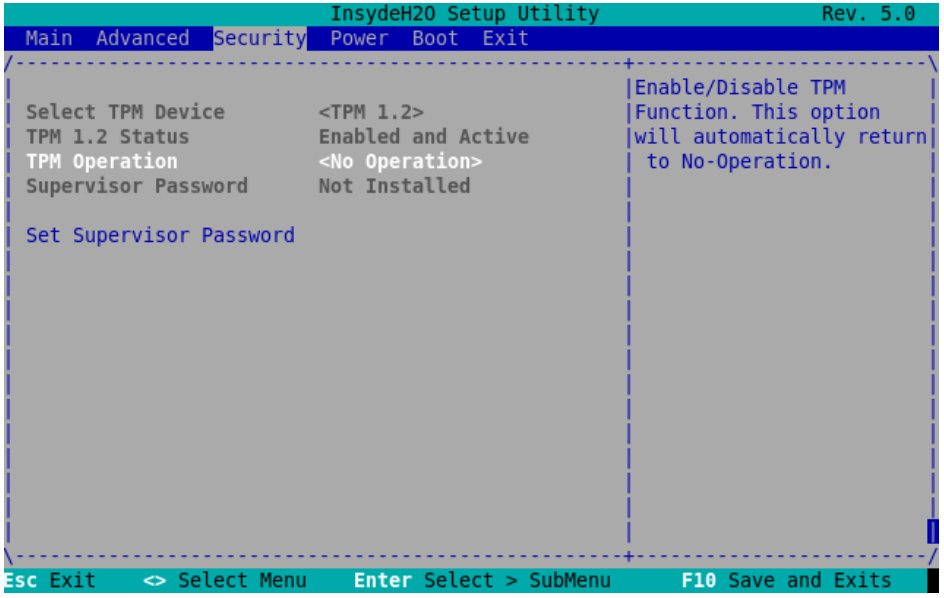
Table 6-16 Advanced >> IPMI Configuration

Item	Values	IPMI Boot Parameter	Description
IPMI KCS Interrupt	Enabled, Disabled	ipmi_irq	Enables/Disables usage of Host Interface (KCS) interrupt. KCS interrupt is hardwired to IRQ 6.
OS Watchdog Timer	Enabled, Disabled	osboot_wd	If enabled, starts the IPMI watchdog just before booting the operating system. The OS has to shut off the watchdog timer when successfully booted.
OS WD Timeout	1, 2, 3, 5, 7, 10, 15, 20 Minutes	osboot_wd_tout	Configure the Timeout of the OS Boot Watchdog Timer.
OS WD Timeout Action	No Action, Hard Reset, Power Down, Power Cycle	osboot_wd_action	Configure how the system should respond if the OS Boot Watchdog Timer expires.
IPMI Fail Safe	Enabled, Disabled, No Change	failsafe	Enables/Disables Fail Safe Policy. Enabled: IPMC will switch the BIOS boot bank if the FRB2 watchdog expires. No Change: Fail Safe Policy will not be changed by BIOS.
Show Sensor Data	--	--	Shows Sensor Data Records (SDR). Lists all SDR information provided by the IPMC.
Execute IPMI Debut Utility	--	--	Executes IPMI Utility for debugging purpose only.

6.7.3 Security

The following table shows the Security menu options.

Figure 6-22 Security



The following table contains information about the options available for Security configuration.

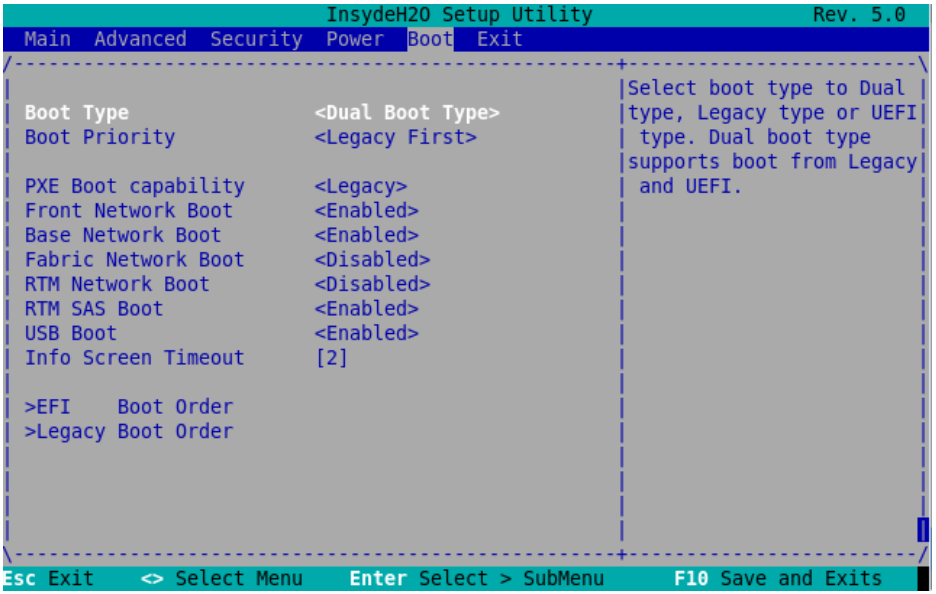
Table 6-17 Security

Item	Values	IPMI Boot Parameter	Description
TPM Operation	No Operation, Disable and Deactivate, Enable and Activate	tpm_operation	Enables/Disables TPM Function. This option will automatically return to No-Operation.
Set Supervisor Password	--	--	Install or Change the password. The length of password must be greater than one character.

6.7.4 Boot

The following figure shows the Boot menu options.

Figure 6-23 Boot



The following table contains information about the options available for Boot configuration.

Table 6-18 Boot

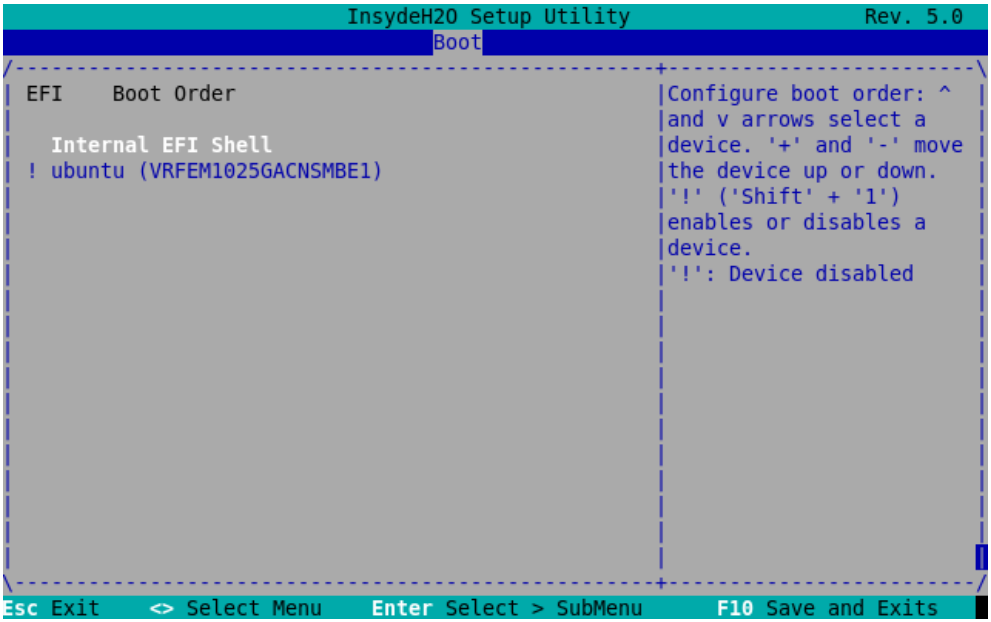
Item	Values	IPMI Boot Parameter	Description
Boot Type	Dual Boot Type, Legacy Boot Type, UEFI boot Type	boot_type	Select boot type to Dual type, Legacy type or UEFI type. Dual boot type supports boot from Legacy and UEFI.
Boot Priority	EFI First, Legacy First	boot_priority	Determine whether EFI devices or Legacy devices are booted first.
PXE Boot capability	Disabled, UEFI:IPv4, UEFI:IPv6, UEFI:IPv4/IPv6, Legacy	boot_netprot	Disabled: Support Network Stack. UEFI PXE: IPv4/IPv6. Legacy: Legacy PXEOPROM only.

Table 6-18 Boot (continued)

Item	Values	IPMI Boot Parameter	Description
Front Panel Net Boot	Enabled, Disabled	boot_frontnet	Controls execution of the Option ROM for the Front Panel Ethernet controller. Select Enabled when Front Panel Boot is required.
Base Network Boot	Enabled, Disabled	boot_basenet	Controls execution of the Option ROM for both Base Network Ethernet controller. Select Enabled when Base Network Boot is required.
Fabric Network Boot	Enabled, Disabled	boot_fabricnet	Controls execution of the Option ROM for all Fabric Network Ethernet controller. Select Enabled when Fabric Network Boot is required.
RTM Network Boot	Enabled, Disabled	boot_rtmnet	Controls execution of the Option ROM for RTM Network Ethernet controller. Select Enabled when RTM Network Boot is required.
RTM SAS Boot	Enabled, Disabled	boot_artmsas	Controls execution of the Option ROM for RTM SAS controller. Select Enabled when RTM SAS Boot is required.
USB Boot	Enabled, Disabled	boot_usb	Disables/Enables booting from USB port devices.
Info Screen Timeout	0 .. 10	info_tmout	The number of seconds that the firmware will wait for <F2> key.

Boot >> EFI Boot Order

Figure 6-24 EFI Boot Order



This menu allows to configure the order of the EFI Boot devices.

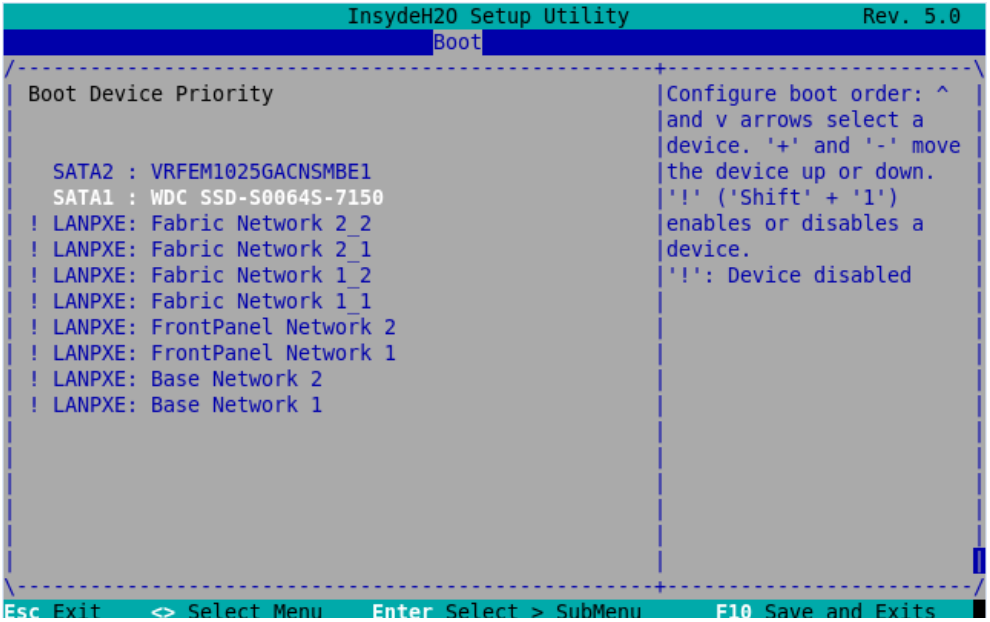
Use the Up and Down keys to select a device.

Use '+' and '-' keys to move the devices up or down.

With the '!' key, a boot device can be enabled or disabled. If the boot entry shows '!' as first character, this boot entry is disabled.

Legacy Boot Order

Figure 6-25 Legacy Boot Order



This menu allows to configure the order of the Legacy Boot devices.

Use the Up and Down keys to select a device.

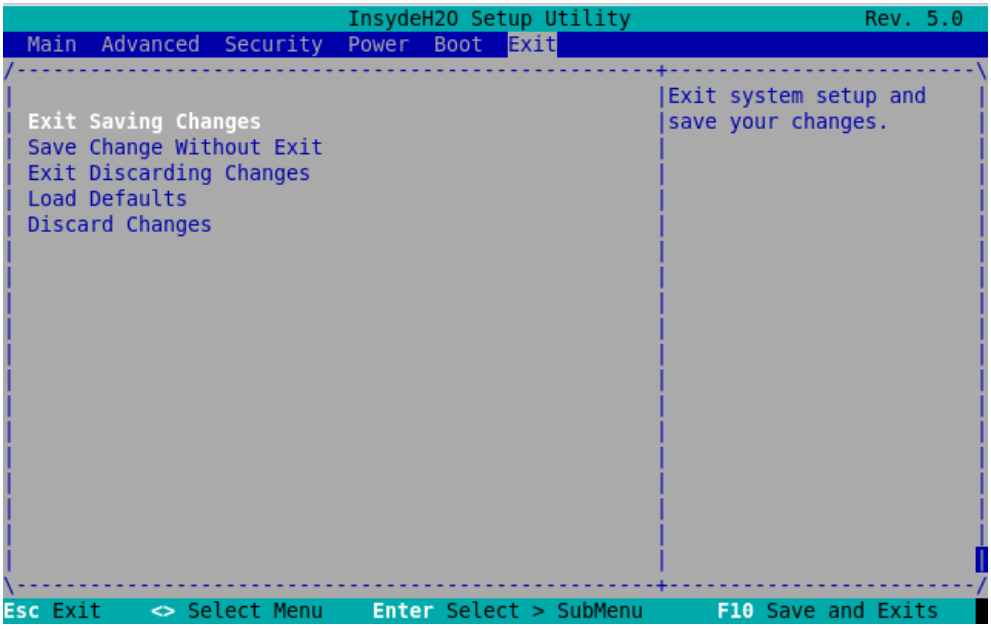
Use '+' and '-' keys to move the devices up or down.

With the '!' key, a boot device can be enabled or disabled. If the boot entry shows '!' as first character, this boot entry is disabled.

6.7.5 Exit

The following figure shows the Exit menu options.

Figure 6-26 Exit Menu



The following table contains information about the options available in Exit menu.

Table 6-19 Exit

Item	Values	IPMI Boot Parameter	Description
Exit Saving Changes	--	--	Saves the changes made and then exits the system.
Save Change Without Exit	--	--	Saves the changes without exiting the system.
Exit Discarding Changes	--	--	Exits the system without saving the changes.
Load Defaults	--	--	Loads default Settings.
Discard Changes	--	--	Discards the changes.

6.8 UEFI Secure Boot

The board is delivered with UEFI Secure Boot option disabled.

To enable the UEFI Secure Boot:

1. Press F2 key to enter BIOS setup. The BIOS boot process starts.
2. Press F4 key during boot process to enter Boot menu.
3. In the Boot menu, select the Administer Secure Boot and press Enter. BIOS restarts the board and enter into the Administer Secure Boot menu.
4. Enable the Restore Secure Boot to Factory Settings setup item. This activatesUEFI Secure Boot.
5. Press F10 key to save the changes.

6.9 Restoring BIOS Default Settings

The blade provides an on-board configuration switch that allows to load BIOS settings from the DEFAULT area of the IPMI Boot Parameters. In order to restore the BIOS default settings using this switch:

1. Remove the blade from the system.
2. Set the on-board switch SW3-4 to ON.
   See *Switch Settings on page 60*, for the exact location of SW3.
3. Install and power up the blade.
4. Wait until the blade has completely booted and is up and running.
5. Remove the blade from the system again.
6. Set switch SW3-4 to OFF.
   Now the BIOS default settings are restored.

6.10 IPMI Support

The ATCA-7480 BIOS provides the following IPMI support:

- Sets initial timestamp for IPMI SEL events.
- Sends Boot Initiated event.
- Sends Memory DIMM detect and error events.
- Sends system firmware progress events.
- Reads IPMC version of the main board and the RTM.

- Reads FRU information of the main board and the RTM.
- Logs boot error in case of no boot device found.
- Reads IPMI GUID and fills in the DMI structure 1 UUID.
- Shows SEL and Sensor Values in BIOS setup.

BIOS creates the DMI structure type 38 to provide IPMI host interface information to the OS.

BIOS reads and creates the IPMI boot parameters, which are stored in the IPMC.

6.11 Watchdog Support

BIOS uses the IPMI payload watchdog for two phases:

- BIOS phase
- Operation System boot phase

The IPMC starts automatically the IPMI payload watchdog after the payload board comes out of reset. In this case, the FRB2 flag of the IPMI watchdog is set.

BIOS can enable the IPMI watchdog to monitor the loading of the operating system. The watchdog starts just before BIOS starts OS boot loader.

The IPMI watchdog can be configured in the BIOS Setup.

6.12 BIOS Error Logging

BIOS supports the following methods to report errors:

- IPMI event logging
- Error logging to the console

6.12.1 Runtime Error Logging

BIOS supports Runtime Error Logging for memory and PCI errors. These errors are logged at BIOS Setup Advanced >> Runtime Error Logging. Errors are logged to the IPMI controller.

Table 6-20 Logged Error Events

Error	IPMI
Correctable: - Correctable ECC Memory Error	Sensor: Memory, Offset 00h

Table 6-20 Logged Error Events (continued)

Error	IPMI
Correctable: - Memory Error Limit Reached - Correctable ECC logging limit reached	Sensor: Memory, Offset 05h
Uncorrectable: - Uncorrectable ECC Memory Error	Sensor: Memory, Offset 01h
PCI PERR	Sensor: Critical Interrupt, Offset 04h PCI PERR
PCI SERR	Sensor: Critical Interrupt, Offset 05h PCI SERR

6.12.2 IPMI Error Logging

BIOS generates status events like Firmware Progress events and error events. The following table shows all BIOS supported IPMI sensors and their possible events.

Table 6-21 BIOS Supported IPMI Events

Sensor	Event
System Firmware Progress (0Fh)	Offset 00h System Firmware Error Supported Event Data2: 00h unspecified Error 01h No system memory 02h No usable system memory 03h SATA device failure 07h No console in found 0Ah No console out found 0Bh Firmware ROM corrupted FDh OEM Error Extension Supported Event Data3 (FDh OEM Error Extension) 21h CPU Built In Self Test (BIST) Error 30h Exception Divide Error 31h Exception Invalid Opcode 32h Exception Stack Fault 33h Exception GP Fault 34h Exception Math Error 35h Exception Alignment Check 36h Exception Machine Check 50h IPMI Boot Parameter Default Area Read Error 51h IPMI Boot Parameter Default Area Locked 52h IPMI Boot Parameter Default Area Checksum Error 53h IPMI Boot Parameter User Area Read Error 54h IPMI Boot Parameter User Area Locked 55h IPMI Boot Parameter User Area Checksum Error 56h IPMI Boot Parameter User Area Write Error 70h Front Panel Network not detected 71h Base Network not detected 72h Fabric Network not detected 73h Accelerator Device not detected 74h RTM SAS Controller not detected 75h RTM Network not detected 76h RTM PCI Bridge not detected 80h Front Panel Network reduced PCI performance

Table 6-21 BIOS Supported IPMI Events (continued)

Sensor	Event
	81h Base Network reduced PCI performance 82h Fabric Network reduced PCI performance 83h Accelerator Device reduced PCI performance 84h RTM SAS Controller reduced PCI performance 85h RTM Network reduced PCI performance 86h RTM PCI Bridge reduced PCI performance Offset 02h System Firmware Progress Supported Event Data2: 01h Memory initialization 02h Hard-Disk (SATA) initialization 03h Secondary processor initialization 04h User authentication 05h User-initiated system setup 06h USB configuration 07h PCI configuration 08h Option ROM initialization 09h Video initialization 0Ah Cache initialization 0Ch Console input initialization 13h Starting Operating System FDh OEM Error Extension Supported Event Data3 (FDh OEM Error Extension) 90h Reboot after a FRB2 Watchdog Timeout 91h Reboot after a BIOS/POST Watchdog Timeout 92h Reboot after a OS Load Watchdog Timeout 93h Reboot after a SMS/OS Watchdog Timeout 94h Reboot after a OEM Watchdog Timeout A0h RTM detected (unknown) A1h RTM-ATCA-747X-10G-SP detected A2h RTM-ATCA-747X-10G-D detected A3h RTM-ATCA-736X-10G-SP detected A4h RTM-ATCA-736X-10G-SAS detected A5h RTM-ATCA-748X-40G detected A6h RTM-ATCA-7360 detected A7h RTM-ATCA-736X-DD detected A8h RTM-ATCA-736X-10G-SP detected AAh RTM-ATCA-736X-10G-SAS detected ABh RTM-ATCA-748X-40G-HA detected ACh SB-RTM451 detected ADh RTM-URA50 detected

Table 6-21 BIOS Supported IPMI Events (continued)

Sensor	Event
Memory (0Ch)	Offset 00h Correctable ECC Offset 01h Uncorrectable ECC Offset 04h Memory Device Disabled Offset 05h Correctable ECC error logging limit reached Offset 06h Presence detected Event Data2: 0xFF Event Data3: **Bit** **Description** 0:3 Sequential DIMM number (1 to 8) 4:7 CPU Socket (1 to 2) See *ATCA-7480 Blade Layout on page 59* for DIMM naming convention.
Critical Interrupt (13h)	Offset 04h PCI PERR Offset 05h PCI SERR Event Data2: Bus number Event Data3: **Bit** **Description** 0:3 PCI Function number 4:7 PCI Device number See *ATCA-7480 Blade Layout on page 59* for DIMM naming convention.
Boot Error (1Eh)	Offset 00h No bootable media (no boot device found)
Battery (29h)	Offset 01h Battery failed

6.13 LED Usage

BIOS uses LED U3 on the front panel to indicate the activity of startup progress. In boot loader phase (PEI phase) U3 is blinking red. In memory initialization phase U3 is blinking amber and in main initialization phase (DXE phase), U3 blinks green. In case of any fatal error, all LEDs U1, U2 and U3 are set to red.

Shortly before closing BIOS and starting an operation system, U3 is switched off.

6.14 Upgrading the BIOS

A BIOS upgrade kit is available for the blade. This allows the BIOS to upgrade. The BIOS upgrade kit contains documentation, which describes in detail how to upgrade the BIOS.

Update tool for Linux is provided with Basic Blade Services (BBS).

The BIOS can also be upgraded via IPMI - HPM.1 (Hardware Platform Management IPM Controller Firmware Upgrade). For more information, refer to the section *Firmware Upgrade on page 285*.

After performing a BIOS upgrade or after restoring a corrupted BIOS image, all BIOS settings are reset to their default values except for parameters that are stored in IPMC storage area.

6.15 BIOS POST Codes

The following table lists the BIOS POST codes. The BIOS POST codes are written to the blade's I/O Port 80 register and can be obtained by reading the "POST code" on-board IPMI sensor. The reading of the "POST code" sensor is only valid when the board is in the BIOS phase. The reading can be used to locate the cause of a board hang during BIOS phase. When the board has booted a OS, the reading of the '"POST code" sensor returns no valid status code.

For debugging purpose, the POST Codes can be printed to the serial console by setting DIP Switch 4-3 and 4-4 to ON.

Table 6-22 BIOS POST Codes

POST Code	Description
02h	Patching CPU microcode
03h	Setup Cache as RAM
04h	PCIE MMIO Base Address initial
05h	CPU Generic MSR initial
06h	Setup CPU speed
07h	Cache as RAM test
08h	Tune CPU frequency ratio to maximum level
09h	Setup BIOS ROM cache

Table 6-22 BIOS POST Codes (continued)

POST Code	Description
0Ah	Enter Boot Firmware Volume
70h	Super I/O initial
71h	CPU Early Initial
72h	Multi-processor Early initial
73h	HyperTransport initial
74h	PCIE MMIO BAR Initial
75h	North Bridge Early Initial
76h	South Bridge Early Initial
77h	PCIE Training
78h	TPM Initial
79h	SMBUS Early Initial
7Ah	Clock Generator Initial
7Bh	Internal Graphic device early initial, PEI_IGDOpRegion
7Ch	HECI Initial
7Dh	Watchdog timer initial
7Eh	Memory Initial for Normal boot
7Fh	Memory Initial for Crisis Recovery
80h	Simple Memory test
81h	TXT function early initial
82h	Start to use Memory
83h	Set cache for physical memory
84h	Recovery device initial
85h	Found Recovery image
86h	Recovery image not found
87h	Load Recovery Image complete
88h	Start Flash BIOS with Recovery image

Table 6-22 BIOS POST Codes (continued)

POST Code	Description
89h	Loading BIOS image to RAM
8Ah	Loading DXE core
8Bh	Enter DXE core
8Ch	iFFS Transition Start
8Dh	iFFS Transition End
40h	TPM initial in DXE
41h	South bridge SPI initial
42h	Setup Reset service, DXE_CF9Reset
43h	South bridge Serial GPIO initial, DXE_SB_SerialGPIO_INIT
44h	Setup SMM ACCESS service
45h	North bridge Middle initial
46h	Super I/O DXE initial
47h	Setup Legacy Region service, DXE_LegacyRegion
48h	South Bridge Middle Initial
49h	Identify Flash device
4Ah	Fault Tolerant Write verification
4Bh	Variable Service Initial
4Ch	Fail to initial Variable Service
4Dh	MTC Initial
4Eh	CPU Middle Initial
4Fh	Multi-processor Middle Initial
50h	SMBUS Driver Initial
51h	8259 Initial
52h	RTC Initial
53h	SATA Controller early initial
54h	Setup SMM Control service, DXE_SMMControler_INIT

Table 6-22 BIOS POST Codes (continued)

POST Code	Description
55h	Setup Legacy Interruput service, DXE_LegacyInterrupt
56h	Relocate SMM BASE
57h	SMI test
58h	VTD Initial
59h	Legacy BIOS initial
5Ah	Legacy interrupt function initial
5Bh	ACPI Table Initial
5Ch	Setup SB SMM Dispatcher service, DXE_SB_Dispatch
5Dh	Setup SB IOTRAP Service
5Eh	Build AMT Table
5Fh	PPM Initial
60h	HECIDRV Initial
61h	Variable store garbage collection and reclaim operation
62h	Do not support flash part (which is defined in SpiDevice.c)
10h	Enter BDS entry
11h	Install Hotkey service
12h	ASF Initial
13h	PCI enumeration
14h	PCI resource assign complete
15h	PCI enumeration complete
16h	Keyboard Controller, Keyboard and Moust initial
17h	Video device initial
18h	Error report device initial
19h	USB host controller initial
1Ah	USB BUS driver initial
1Bh	USB device driver initial

Table 6-22 BIOS POST Codes (continued)

POST Code	Description
1Ch	Console device initial fail
1Dh	Display logo or system information
1Eh	IDE controller initial
1Fh	SATA controller initial
20h	SIO controller initial
21h	ISA BUS driver initial
22h	Floppy device initial
23h	Serial device initial
24h	IDE device initial
25h	AHCI device initial
26h	Dispatch option ROMs
27h	Get boot device information
28h	End of boot selection
29h	Enter Setup Menu
2Ah	Enter Boot manager
2Bh	Try to boot system to OS
2Ch	Shadow Misc Option ROM
2Dh	Save S3 resume required data in RAM
2Eh	Last Chipset initial before boot to OS
2Fh	Start to boot Legacy OS
30h	Start to boot UEFI OS
31h	Prepare to Boot to Legacy OS
32h	Send END of POST Message to ME via HECI
33h	Last Chipset initial before boot to Legacy OS
34h	Ready to Boot Legacy OS
35h	Fast recovery start flash

Table 6-22 BIOS POST Codes (continued)

POST Code	Description
36h	SDHC device initial
37h	Ata Legacy device initial
38h	SD Legacy device initial
F9h	No Boot Device, PostBDS_NO_BOOT_DEVICE
FBh	UEFI Boot Start Image, PostBDS_START_IMAGE
FDh	Legacy 16 boot entry
FEh	Try to Boot with INT 19
A0h	Identify Flash device in SMM
A2h	SMM service initial
A6h	OS call ACPI enable function
A7h	ACPI enable function complete
A1h	Enter S1
A3h	Enter S3
A4h	Enter S4
A5h	Enter S5
A8h	OS call ACPI disable function
A9h	ACPI disable function complete
C0h	Memory initial for S3 resume
C1h	Get S3 resume required data from memory
C2h	Start to use memory during S3 resume
C3h	Set cache for physical memory during S3 resume
C4h	Start to restore system configuration
C5h	Restore system configuration stage 1
C6h	Restore system configuration stage 2
C7h	Relocate SMM BASE during S3 resume
C8h	Multi-processor initial during S3 resume

Table 6-22 BIOS POST Codes (continued)

POST Code	Description
C9h	Start to restore system configuration in SMM
CAh	Restore system configuration in SMM complete
CBh	Back to OS
51h	Prepare to enter S1
53h	Prepare to enter S3
54h	Prepare to enter S4
55h	Prepare to enter S5
E1h	System wakeup from S1
E3h	System wakeup from S3
E4h	System wakeup from S4
E5h	System wakeup from S5
A0h	QPI Initialization: Initialize QPI inuput structure default values
A1h	QPI Initialization: Collect info such as SBSP, Boot Mode, Reset type and so on.
A2h	QPI Initialization: Setup IO SADs in SBSP to access the config space
A3h	QPI Initialization: Setup up minimum path between SBSP & other sockets
A4h	QPI Initialization: Setup IO SADs in PBSP to access the config space
A5h	QPI Initialization: System configurations that require some kind of reset
A6h	QPI Initialization: Sync up with PBSPs
A7h	QPI Initialization: Topology discovery and route calculation
A8h	QPI Initialization: Program final route
A9h	QPI Initialization: Program final IO SAD setting
AAh	QPI Initialization: Protocol layer and other Uncore settings
ABh	QPI Initialization: Transition links to full speed operation
ACh	QPI Initialization: Phy layer settings
ADh	QPI Initialization: Link layer settings
AEh	QPI Initialization: Coherency Settings

Table 6-22 BIOS POST Codes (continued)

POST Code	Description
AFh	QPI Initialization: QPI is done
B0h	Memory Initialization: DIMM Detect
B1h	Memory Initialization: Clock
B2h	Memory Initialization: Read SPD data
B3h	Memory Initialization: Early Init
B4h	Memory Initialization: Rank Detection
B5h	Memory Initialization: Early Channel Init
B6h	Memory Initialization: JEDEC Init
B7h	Memory Initialization: Channel Training
B8h	Memory Initialization: Throttling Init
B9h	Memory Initialization: BIST
BAh	Memory Initialization: Init
BBh	Memory Initialization: DDR Memory Mapping
BCh	Memory Initialization: RAS Configuration
BDh	Memory Initialization: Get Margins
BFh	Memory Initialization: MRC Done

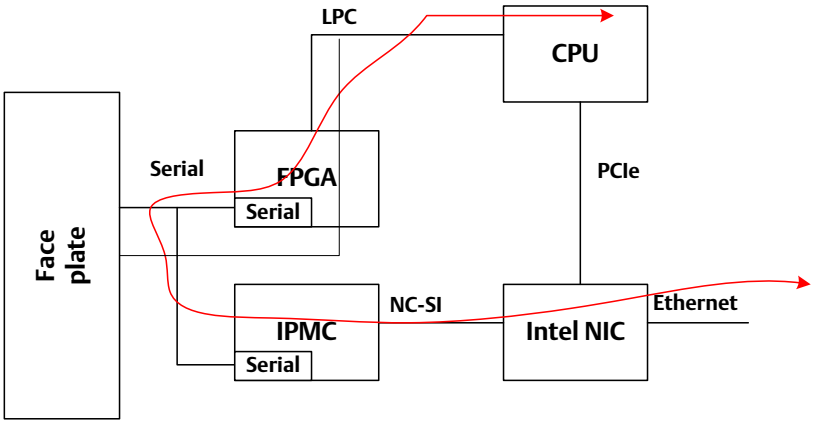
Serial Over LAN

7.1 Overview

Serial Over LAN (SOL) is a mechanism that you can use to redirect the serial console from the blade via an IPMI session over the network. SOL uses the RMCP+ protocol.

The IPMC is used to establish and control the SOL session. Only SOL is available on the base interface. The sideband interface of the Intel NIC is used to transmit/receive its terminal characters via base interface.

Figure 7-1 SOL Overview



You can configure the SOL parameters via standard IPMI commands or via an open source tool called ipmitool.

The ATCA-7480 supports two SOL channels, which are available at their base interfaces. However, only one SOL session is allowed at a time.

Table 7-1 SOL Channels

SOL/LAN Channel #	Ethernet Device	
1	base1	SOL Channel #1 at Base Interface #1
2	base2	SOL Channel #2 at Base Interface #2

7.2 Installing the ipmitool

You can download the open source tool ipmitool from *http://ipmitool.sourceforge.net* (at the time of publishing this manual the current version is 1.8.13). Documentation for this tool is also freely available on this site.

Procedure

To install the ipmitool:

1. Download the ipmitool tar file from *http://ipmitool.sourceforge.net* to your blade.
2. Extract the source code.
   `prompt>tar -xjvf ipmitool-<version>.tar.bz2`
3. Go to the directory where ipmitool is extracted.
   `prompt>cd <path>/ipmitool-<version>`
4. Build the ipmitool.
   `prompt>./configure && make && make install`

7.3 Configuring SOL Parameters

You can configure the following SOL parameters.

Table 7-2 SOL Parameters

Parameter	Description
Set LAN Configuration Parameter (IP address/MAC address)	Use this command to set the IP and MAC address.
Set Channel Access (Privilege level)	Use this command to set the privilege level.
Set User Name	Default value is soluser.
Set User Password	Default value is solpasswd.

You can use standard IPMI commands or the ipmitool to modify the parameters.

7.3.1 Using Standard IPMI Commands

This example shows how to setup the SOL configuration parameter with standard IPMI commands. `ipmicmd` is used on the local IPMC and the IP is configured.

Sample Procedure

To set the IP address:

1. Establish an IPMI connection to the blade.
2. Set LAN Configuration Parameter Set In Progress Lock.
   ipmicmd -k "f 0 c 1 1 0 1" smi 0
3. Set LAN Configuration Parameter Set IP (172.16.10.11 on channel 5).
   ipmicmd -k "f 0 c 1 1 3 ac 10 0a dd" smi 0
4. Set LAN Configuration Parameter Set In Progress Commit.
   ipmicmd -k "f 0 c 1 1 0 2" smi 0

7.3.2 Using ipmitool

The example below shows how to setup a LAN configuration parameter for a potential SOL session with ipmitool for base 0 (channel 5).

```
n0s70:~ # ipmitool lan set 1 ipaddr 172.16.0.221
Setting LAN IP Address to 172.16.0.221
n0s70:~ #
```

The following example shows how to query the LAN parameters that are currently in use for a potential SOL session for base 0 (channel 1) and base 1 (channel 2):

```
root@localhost:~# ipmitool lan print 1
Set in Progress         : Set Complete
Auth Type Support       :
Auth Type Enable        : Callback :
                        : User     :
                        : Operator :
                        : Admin    :
                        : OEM      :
IP Address Source       : Unspecified
IP Address              : 172.16.0.221
Subnet Mask             : 255.255.0.0
MAC Address             : ec:9e:cd:10:a0:64
Default Gateway IP      : 172.16.0.1
```

```
Default Gateway MAC     : 00:00:00:00:00:00
RMCP+ Cipher Suites     : 1,2,3,3
Cipher Suite Priv Max   : Not Available
root@localhost:~# ipmitool lan print 2
Set in Progress         : Set Complete
Auth Type Support       :
Auth Type Enable        : Callback :
                        : User     :
                        : Operator :
                        : Admin    :
                        : OEM      :
IP Address Source       : Unspecified
IP Address              : 172.17.1.220
Subnet Mask             : 255.255.0.0
MAC Address             : ec:9e:cd:10:a0:65
Default Gateway IP      : 172.17.0.1
Default Gateway MAC     : 00:00:00:00:00:00
RMCP+ Cipher Suites     : 1,2,3,3
Cipher Suite Priv Max   : Not Available
root@localhost:~#
```

7.4 Establishing an SOL Session

Procedure

To establish a SOL session:

1. Make sure that the requirements detailed above are fulfilled.
2. Compile and install the ipmitool on your target, which is destined for opening the SOL session on the ATCA-7480. For details refer to *Installing the ipmitool on page 226*.
3. Apply an IP address to the ATCA-7480 SOL interface. For details, see to *Configuring SOL Parameters on page 226*.

4. Change user and password, if necessary. Default user is "soluser" and password is "solpasswd".
5. Configure the network between the ATCA-7480 Series and your target, which is destined for opening the SOL session, so that the SOL IP address is accessible.
6. Start ATCA-7480 Series SOL session on your target with the ipmitool and the configured IP address for the ATCA-7480 SOL interface.

   ```
   ipmitool -C 1 -I lanplus -H 172.16.0.221 -U soluser -P solpasswd -
   k gkey sol activate
   ```

For details on the command parameters, refer to the ipmitool documentation available on *http://ipmitool.sourceforge.net*.

To see the BIOS serial interface in SOL Session operational, use ~? for help. It might be necessary to write a logical "1" into FPGA register offset 0x04 (ipmicmd -k "f 0 6 52 1 fe 0 4 1" smi 0) - This is needed with BIOS version prototypes.

Supported IPMI Commands

8.1 Standard IPMI Commands

The IPMC is fully compliant to the Intelligent Platform Management Interface v1.5. This section provides information about the supported IPMI commands.

8.1.1 Global IPMI Commands

The IPMC supports the following global IPMI commands.

Table 8-1 Supported Global IPMI Commands

Command	NetFn (Request/Response)	CMD	Comments
Get Device ID	0x06/0x07	0x01	-
Cold Reset	0x06/0x07	0x02	-
Warm Reset	0x06/0x07	0x03	-
Get Self Test Results	0x06/0x07	0x04	-
Get Device GUID	0x06/0x07	0x08	-
Master Write-Read	0x06/0x07	0x52	Only for accessing private I^2C buses.

8.1.2 System Interface Commands

The system interface commands are supported by blades providing a system interface.

Table 8-2 Supported System Interface Commands

Command	NetFn (Request/Response)	CMD
Set BMC Global Enables	0x06/0x07	0x2E
Get BMC Global Enables	0x06/0x07	0x2F
Clear Message Flags	0x06/0x07	0x30
Get Message Flags	0x06/0x07	0x31
Get Message	0x06/0x07	0x33
Send Message	0x06/0x07	0x34

Table 8-2 Supported System Interface Commands (continued)

Command	NetFn (Request/Response)	CMD
Set Channel Access	0x06/0x07	0x40
Get Channel Access	0x06/0x07	0x41
Get Channel Info	0x06/0x07	0x42
Set User Access	0x06/0x07	0x43
Get User Access	0x06/0x07	0x44
Set User Name	0x06/0x07	0x45
Get User Name	0x06/0x07	0x46
Set User Password	0x06/0x07	0x47
Set User Payload Access	0x06/0x07	0x4C
Get User Payload Access	0x06/0x07	0x4D
Set Channel Security Keys	0x06/0x07	0x5C

8.1.3 Watchdog Commands

The watchdog commands are supported by the blades providing a system interface and a watchdog type 2 sensor.

The pre-timeout and power-cycle options are not supported.

Table 8-3 Supported Watchdog Commands

Command	NetFn (Request/Response)	CMD
Reset Watchdog Timer	0x06/0x07	0x22
Set Watchdog Timer	0x06/0x07	0x24
Get Watchdog Timer	0x06/0x07	0x25

8.1.4 SEL Device Commands

Table 8-4 Supported SEL Device Commands

Command	NetFn (Request/Response)	CMD
Get SEL Info	0x0A/0x0B	0x40
Reserve SEL	0x0A/0x0B	0x42
Get SEL Entry	0x0A/0x0B	0x43
Add SEL Entry	0x0A/0x0B	0x44
Clear SEL	0x0A/0x0B	0x47
Get SEL Time	0x0A/0x0B	0x48
Set SEL Time	0x0A/0x0B	0x49

8.1.5 FRU Inventory Commands

Table 8-5 Supported FRU Inventory Commands

Command	NetFn (Request/Response)	CMD
Get FRU Inventory Area Info	0x0A/0x0B	0x10
Read FRU Data	0x0A/0x0B	0x11
Write FRU Data	0x0A/0x0B	0x12

8.1.6 Sensor Device Commands

Table 8-6 Supported Sensor Device Commands

Command	NetFn (Request/Response)	CMD	Comments
Get Device SDR Info	0x04/0x05	0x20	-
Get Device SDR	0x04/0x05	0x21	-
Reserve Device SDR Repository	0x04/0x05	0x22	-

Table 8-6 Supported Sensor Device Commands (continued)

Command	NetFn (Request/Response)	CMD	Comments
Get Sensor Reading Factors	0x04/0x05	0x23	-
Set Sensor Hysteresis	0x04/0x05	0x24	-
Get Sensor Hysteresis	0x04/0x05	0x25	-
Set Sensor Threshold	0x04/0x05	0x26	Most of the threshold-based sensors have fixed thresholds. Before using this command, check whether threshold setting is supported by using the Get Device SDR command.
Get Sensor Threshold	0x04/0x05	0x27	-
Set Sensor Event Enable	0x04/0x05	0x28	-
Get Sensor Event Enable	0x04/0x05	0x29	-
Get Sensor Event Status	0x04/0x05	0x2B	-
Get Sensor Reading	0x04/0x05	0x2D	-
Get Sensor Type	0x04/0x05	0x2F	-
Set Event Receiver	0x04/0x05	0x00	-
Get Event Receiver	0x04/0x05	0x01	-
Platform Event	0x04/0x05	0x02	-

8.1.7 Chassis Device Commands

Table 8-7 Supported Chassis Device Commands

Command	NetFn (Request/Response)	CMD
Set System Boot Options	0x00/0x01	0x08
Get System Boot Options	0x00/0x01	0x09

8.1.7.1 System Boot Options Commands

The IPMI system boot options commands allow you to control the boot process of a blade by sending boot parameters to the blade's boot firmware (for example BIOS, U-Boot or VxWorks). The boot firmware interprets the sent boot parameters and executes the boot process accordingly. Each boot parameter addresses a particular functionality and consists of a sequence of one or more bytes. The IPMI specification assigns numbers to boot parameters. Boot parameters 0 to 7 are standard parameters whose structure and functionality is defined by the IPMI specification. The boot parameters 96 to 127 are OEM-specific which can be used for different purposes.

When using the Get/Set System Boot Options commands, except for parameter 100, use the response/request data fields with the Set Selector and the Block Selector set to 0x00. When using the Get/Set System Boot Option for the parameter 100, the Set Selector and the Block Selector have a specific meaning. For more details, see *System Boot Options Parameter #100 on page 237* for details.

The following table lists boot properties that can be configured and their corresponding boot parameter numbers.

Table 8-8 Configurable System Boot Option Parameters

Configurable Boot Property	Corresponding Boot Parameter Number
Selection between default and backup boot flash as device to boot from Selection between default and backup EEPROM as device where the on-board FPGA loads its configuration stream from	96
Timeout for graceful shutdown	98
BIOS boot parameters	100

8.1.7.1.1 System Boot Options Parameter #96

This boot parameter is a Penguin Edge specific OEM boot parameter. Its definition is given in the following table.

Table 8-9 System Boot Options Parameter #96

Data Byte	Description
1	Bits 7:2: Reserved
	Bit 1: FPGA configuration stream load 0: Load configuration stream from default boot flash 1: Load configuration stream from backup boot flash **Note:** The new FPGA configuration stream is loaded into the FPGA at the next power-up of the payload.
	Bit 0: Default/backup boot flash selection 0: Boot from default boot flash 1: Boot from backup boot flash **Note**: The newly selected boot flash is connected to the payload immediately, which means that the writing to the flash is possible. Its image is executed after the next power-up or cold reset of the payload.

The System Boot Options parameter #96 is non-volatile. During blade production, its data is initialized to 0xFF and its state is set to invalid. Its parameter data remains preserved after IPMC power cycles and firmware upgrades.

8.1.7.1.2 System Boot Options Parameter #98

This boot parameter is a Penguin Edge specific OEM parameter. This timer specifies how long the IPMC waits for the payload to shut down. If the payload software does not configure its OpenIPMI library to be notified for shutdown requests, the IPMC shuts down the payload when the timer expires.

Table 8-10 System Boot Options Parameter #98

Bit	Description
15:8	Timeout for GRACEFUL_SHUTDOWN, LSB (given in 100msec)
7:0	Timeout for GRACEFUL_SHUTDOWN, MSB (given in100 msec)

The System Boot Options parameter #98 is non-volatile. During blade production its data is initialized to 0xFF and its state is set to invalid. Its parameter data remains preserved after IPMC power cycles and firmware upgrades.

8.1.7.1.3 System Boot Options Parameter #100

The system boot options parameter #100 allows you to send multiple boot options to the blade's boot firmware and thus control the boot process. The boot options which you can configure using this parameter are typically a subset of the boot options which you can configure in the boot firmware directly, for example, using a Setup menu.

The IPMC contains a storage area where the boot parameters are stored. When the blade boots, the boot firmware reads out the storage area, interprets the parameters and executes the boot process accordingly.

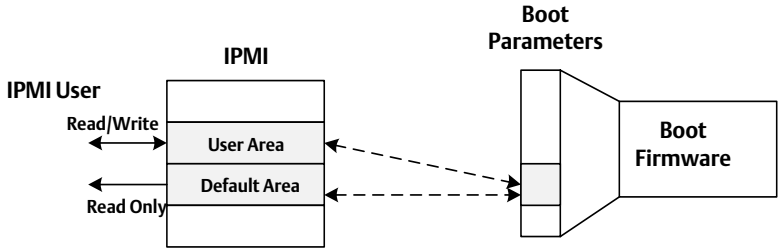
NOTICE
The boot parameters in the IPMC storage area have higher priority than the same boot options, which may be configured in the firmware itself, for example, using the setup menu.

The storage area is divided into two parts: the default area and the user area. The user area can be read and written by an IPMI user and default is, the area which the boot firmware reads out and uses during the boot process. The default area can only be read by both the IPMI user and the boot firmware. Its purpose is to store factory-programmed default boot options which can be used to restore the standard settings. If you want the boot firmware to read out and use the boot parameters stored in the default area and thus use the factory settings, you need to configure the blade accordingly. This is typically done by an on-board switch (for example, Clear CMOS RAM"). It depends on the blade and firmware which settings are stored in the default area. The details are given in the following sections.

On some blades with particular firmware types, changing a boot parameter in the firmware setup menu changes the boot parameter in the user area as well, if the same parameter is defined both in the user area and the set-up menu.

The following figure summarizes the previously explained basic information flow related to the system boot options parameter #100.

Figure 8-1 System Boot Options Parameter #100 - Information Flow Overview



The boot options need to be stored as a sequence of zero terminated strings. The following table describes in detail the format of the boot options to be used when setting or reading the System Boot Options parameter #100.

Table 8-11 System Boot Options - Parameter #100 - Data Format

Byte	Description
0..1	Number of bytes used for boot parameters (LSB first) The number of bytes must be calculated and written into these two bytes by the software which writes into the storage area. The values 0x0000 and 0xFFFF indicate that no data has been written to the storage area. When reading from the storage area and you find any of these two values, your software should assume that no user-specific boot options have previously been written to the storage area.
2 .. n	Boot parameters data The boot parameters are stored as ASCII text with the following general format: <name>=<value>, where all name/value pairs are separated by a zero byte. The end of the boot parameter data is indicated by two zero bytes. Allowed and supported name/value pairs are blade-specific.
n + 1 .. n + 2	16 byte checksum over the boot parameters data section. (LSB first) For backward compatibility reasons, the checksums 0x0000 and 0xFFFF are accepted as valid. They indicate that no checksum has been calculated and stored.

When writing to or reading from the storage area, you can only read or write chunks of 16 bytes at a time. For this reason, the default and user area are divided into numbered blocks of 16 bytes which need to be addressed individually. For this purpose, the "Block Selector" field in the request data field is used. The "Set Selector" field, on the other hand, is used to select either the default or user area.

The following two tables describe in detail how the request and response data fields need to be filled and interpreted when performing SET and GET accesses.

Table 8-12 System Boot Options Parameter #100 - SET Command Usage

Byte	Description
Request Data	
1	Bit 7: when set to "1", the storage area on the IPMC is locked, i.e. no other software can access it. This should be set, before doing any modifications and cleared again after the final access. Bits 6..0: must contain the value: "100", indicating this OEM system boot option.
2	Set Selector Must be set to "0" (user area). You can only write to the user area, therefore no other values are supported.
3	Block Selector Zero based index of the 16-byte block which you want to write to. Index 0 refers to the first block of 16 bytes, which includes the first two bytes that indicate the boot parameter data size. Depending on the total length of the boot option data, your software may need to write several blocks of 16 bytes in a row, each individually addressed using the block selector.
4 .. n (n <= 19)	Data that you want to write into the addressed block. This will be a chunk of the boot parameter data. If less than 16 bytes are written, then only the provided data is written, the remaining bytes in the addressed storage area block are left unchanged.
Response Data	
1	0x00: Write successful 0x80: Boot parameter storage not supported by the IPMC 0x81: Storage area is locked by another software entity 0x82: Illegal write-access 0xC9: Block selector is outside of the allowed range.

Table 8-13 System Boot Options Parameter #100 - GET Command Usage

Byte	Description
Request Data	
1	Bit 7: reserved. Set to "0". Bits 6..0: must contain the value: "100", indicating this OEM system boot option.
2	Set Selector 0: User area 1: Default area
3	Block Selector Zero based index of the 16-byte block which you want to read from. Index 0 refers to the first block of 16 bytes, which includes the first two bytes which indicate the boot parameter data size.
Response Data	
1	0x00: Read successful 0x80: Boot parameter storage not supported by the IPMC 0xC9: Block selector is outside of the allowed range.
2	Reserved. Set to "1".
3	Bit 7: If set to "1", the addressed storage area is locked. Bits 6 ..0: value "100", indicating this OEM boot option command.
4 .. 19	The content of the read 16-byte block.

In order to detect the maximum size of writable storage area, your software can perform a series of read accesses while incrementing the block selector with each access. Once the error code C9 is returned, the limit has been reached and the total available space in the writable storage area can be easily determined by the number of previously performed successful read accesses.

This is supported by HPI, for details refer to the *System Management Interface Based on HPI-B User's Guide* related to your system environment.

Penguin Edge provides the tool ipmibpar to interpret the ASCII parameters. To obtain the tool, contact your local sales representative.

Table 8-14 System Boot Options Parameter #100 - Supported Parameters

Parameter	Description	Values
rtm_auto	If enabled, the RTM is detected and the RTM PCIe parameter are set for this RTM. If disabled, the RTM PCIe parameter can be set manually.	on off
rtm_cpu0_bif	Selects CPU0 PCIe Bifurcation for Zone 3 connector (RTM)	X4x4x4x4 x4x4x8 x8x4x4 x8x8
rtm_cpu0_3a	Selects CPU0 PCIe Port 3A Speed for Zone 3 connector (RTM)	auto gen1 gen2 gen3
rtm_cpu0_3b	Selects CPU0 PCIe Port 3B Speed for Zone 3 connector (RTM)	auto gen1 gen2 gen3
rtm_cpu0_3c	Selects CPU0 PCIe Port 3C Speed for Zone 3 connector (RTM)	auto gen1 gen2 gen3
rtm_cpu0_3d	Selects CPU0 PCIe Port 3D Speed for Zone 3 connector (RTM)	auto gen1 gen2 gen3
rtm_cpu1_bif	Selects CPU1 PCIe Bifurcation for Zone 3 connector (RTM)	X4x4x4x4 x4x4x8 x8x4x4 x8x8 x16

Table 8-14 System Boot Options Parameter #100 - Supported Parameters (continued)

Parameter	Description	Values
rtm_cpu1_3a	Selects CPU1 PCIe Port 3A Speed for Zone 3 connector (RTM)	auto gen1 gen2 gen3
rtm_cpu1_3b	Selects CPU1 PCIe Port 3B Speed for Zone 3 connector (RTM)	auto gen1 gen2 gen3
rtm_cpu1_3c	Selects CPU1 PCIe Port 3C Speed for Zone 3 connector (RTM)	auto gen1 gen2 gen3
rtm_cpu1_3d	Selects CPU1 PCIe Port 3D Speed for Zone 3 connector (RTM)	auto gen1 gen2 gen3
frontnet	Enable/Disable Front Panel Ethernet	on off
pci_sriov	PCI Express Single Root I/O Virtualization	on off
pci_ari	Alternative Routing ID nterpretation (ARI)	on off
pci_64bit	64-bit BAR support for PCI devices	on off
clock_ssc	Spread Spectrum Clock	on off
vtd	Intel Virtualization Technology for Directed I/O (VT-d)	on off
vtd_ir	VT-d Interrupt Remapping Support	on off

Table 8-14 System Boot Options Parameter #100 - Supported Parameters (continued)

Parameter	Description	Values
sata	SATA controller Operation Mode	on off
sata_alpm	Aggressive Link Power Management (SALP)	on off
sata_mode	SATA Controller Operation Mode	ide ahci raid
sata_raidwait	Delay of SATA RAID Option ROM prompt in Seconds	2 4 6 8
sata_speed	Maximum SATA speed	1.5 3 6
usb	USB Support	on off uefi
usb1	Enable/Disable USB Front Panel Port 1	on off
usb2	Enable/Disable USB Front Panel Port 2	on off
usb_rtm	Enable/Disable USB to RTM	on off
usb1_3	USB1 Front Panel USB 3.0 support	on off
usb2_3	USB2 Front Panel USB 3.0 support	on off
cpu0_dism	Core Disable Bitmap Hex Value. 0: Enable all cores. Valid Range: 0 to 3FFE. 3FFF=Disabling all cores: Invalid	Hex Value 0 to 3FFE

Table 8-14 System Boot Options Parameter #100 - Supported Parameters (continued)

Parameter	Description	Values
cpu1_dism	Core Disable Bitmap Hex Value. 0: Enable all cores. Valid Range: 0 to 3FFE. 3FFF=Disabling all cores: Invalid	Hex Value 0 to 3FFE
cpu_ht	CPU Hyper Threading	on off
cpu_ed	CPU Execute Disable	on off
cpu_txt	Intel Trusted Execution Technology (TXT).	on off
cpu_vt	CPU Virtualization (VT-x)	on off
cpu_hp	CPU Hardware Prefetcher	on off
cpu_acp	CPU Adjacent Cache Prefetcher	on off
cpu_dca	CPU Direct Cache Access (DCA)	on off
cpu_x2apic	CPU Extended APIC support	on off
cpu_ss	CPU Enhanced Intel SpeedStep Technology (P-States).	on off
cpu_tm	CPU Turbo Mode	on off
cpu_ppw	Turbo Mode Performance/Watt	tradi optim
cpu_cstates	CPU C-State support	on off

Table 8-14 System Boot Options Parameter #100 - Supported Parameters (continued)

Parameter	Description	Values
cpu_cslimit	Package C State limit	c0c1 c2 c6nr c6r no
cpu_c3	CPU C3 report	on off
cpu_c6	CPU C6 report	on off
cpu_c1e	CPU Enhanced Halt State (C1E)	on off
cpu_cxacpi	Report ACPI Cx State	c2 c3
mem_speed	Memory Frequency (MHz)	auto 1333 1600 1867 2133
mem_halt	Halt on Training Error	on off
mem_numa	Disable Non Uniform Memory Access (NUMA).	on off
mem_test	Hardware Memory Test	off short long
mem_ras	Memory RAS modes	off mirror lockstep
mem_sparing	Memory Rank Sparing	on off

Table 8-14 System Boot Options Parameter #100 - Supported Parameters (continued)

Parameter	Description	Values
mem_ps	Memory Patrol Scrub	on off
mem_ds	Memory Demand Scrub	on off
con_tt	Serial console terminal type	vt100 vt100+ utf8 ansi
con_br	Serial console baud rate	9600 19200 38400 57600 115200
con_db	Serial console data bits	7 8
con_par	Serial console parity bits	o e o
con_sb	Serial console stop bits	1 2
con_fc	Serial console flow control	off hard soft
con_ap	Serial console redirection after POST	on off
apei	APEI Support	on off
apei_uefiver	UEFI revision of APEI error format	uefi22 uefi23

Table 8-14 System Boot Options Parameter #100 - Supported Parameters (continued)

Parameter	Description	Values
ipmi_irq	IPMI KCS Interrupt	on off
osboot_wd	OS Watchdog Timer	on off
osboot_wd_tout	0S Watchdog Timeout in minutes	1 2 3 5 7 10 15 20
osboot_wd_action	0S Watchdog Timeout Action	noaction reset poweroff powercycle
failsafe	IPMI Fail Safe	on off nochange
tpm_operation	TPM Function. This option will automatically return to No-Operation.	no_operation disable_deactivate enable_activate
boot_type	Boot Type	dual legacy uefi
boot_priority	Determine whether EFI devices or Legacy devices are booted first	uefi legacy
boot_netprot	PXE Boot capability	ipv4 ipv6 ipv4v6 legacy

Table 8-14 System Boot Options Parameter #100 - Supported Parameters (continued)

Parameter	Description	Values
boot_frontnet	Front Panel Net Boot	on off
boot_basenet	Base Network Boot	on off
boot_fabricnet	Fabric Network Boot	on off
boot_rtmnet	RTM Network Boot	on off
boot_artmsas	RTM SAS disk Boot	on off
boot_usb	USB device boot	on off
info_tmout	The number of seconds that the firmware will wait for <F2> key	on off
boot_order	Set the Boot Order See *Table 8-15*.	device1… deviceN separated by comma

Table 8-15 Boot Order Devices

Boot Device	Description
sata0	On-board SATA device (P1)
sata1	On-board SATA device (P2)
sata2	On-board SATA device (P3)
sata3	SATA device RTM
raid0	SATA RAID device 0
raid1	SATA RAID device 0
raid2	SATA RAID device 0

Table 8-15 Boot Order Devices (continued)

Boot Device	Description
raid3	SATA RAID device 0
sashdd	RTM SAS HDD
sas_NNN	SAS Controller NNN = SCSI ID (use this when using an SAS array)
frontnet1	Front Panel Network 1
frontnet2	Front Panel Network 2
basenet1	Base Network 1
basenet2	Base Network 2
fabricnet11	Fabric Network 1_1
fabricnet12	Fabric Network 1_2
fabricnet21	Fabric Network 2_1
fabricnet22	Fabric Network 2_2
rtmnet1	RTM Network 1
rtmnet2	RTM Network 2
rtmnet3	RTM Network 3
rtmnet4	RTM Network 4
rtmnet5	RTM Network 5
rtmnet6	RTM Network 6
rtmnet7	RTM Network 7
rtmnet8	RTM Network 8
rtmnet9	RTM Network 9
rtmnet10	RTM Network 10
usbcdrom	USB CDROM/DVDROM

Table 8-15 Boot Order Devices (continued)

Boot Device	Description
usbcdrom1	USB CDROM/DVDROM connected to USB1
usbcdrom2	USB CDROM/DVDROM connected to USB2
usbcdrom3	USB CDROM/DVDROM connected to USB RTM
usbhdd	USB HDD
usbhdd1	USB HDD connected to USB1
usbhdd2	USB HDD connected to USB2
usbhdd3	USB HDD connected to USB RTM
usbfdd	USB Floppy disk
eiffrontnet1	EFI Front Panel Network 1 (IPv4)
efifrontnet2	EFI Front Panel Network 2 (IPv4)
efibasenet1	EFI Base Network 1 (IPv4)
efibasenet2	EFI Base Network 2 (IPv4)
efifabricnet11	EFI Fabric Network 1_1 (IPv4)
efiffabricnet12	EFI Fabric Network 1_2 (IPv4)
efifabricnet21	EFI Fabric Network 2_1 (IPv4)
efifabricnet22	EFI Fabric Network 2_2 (IPv4)
efirtmnet1	EFI RTM Network 1 (IPv4)
efirtmnet2	EFI RTM Network 2 (IPv4)
efirtmnet3	EFI RTM Network 3 (IPv4)
efirtmnet4	EFI RTM Network 4 (IPv4)
efirtmnet5	EFI RTM Network 5 (IPv4)
efirtmnet6	EFI RTM Network 6 (IPv4)

Table 8-15 Boot Order Devices (continued)

Boot Device	Description
efirtmnet7	EFI RTM Network 7 (IPv4)
efirtmnet8	EFI RTM Network 8 (IPv4)
efirtmnet9	EFI RTM Network 9 (IPv4)
efirtmnet10	EFI RTM Network 10 (IPv4)
eiffrontnet1v6	EFI Front Panel Network 1 (IPv6)
efifrontnet2v6	EFI Front Panel Network 2 (IPv6)
efibasenet1v6	EFI Base Network 1 (IPv6)
efibasenet2v6	EFI Base Network 2 (IPv6)
efifabricnet11v6	EFI Fabric Network 1_1 (IPv6)
efiffabricnet12v6	EFI Fabric Network 1_2 (IPv6)
efifabricnet21v6	EFI Fabric Network 2_1 (IPv6)
efifabricnet22v6	EFI Fabric Network 2_2 (IPv6)
efirtmnet1v6	EFI RTM Network 1 (IPv6)
efirtmnet2v6	EFI RTM Network 2 (IPv6)
efirtmnet3v6	EFI RTM Network 3 (IPv6)
efirtmnet4v6	EFI RTM Network 4 (IPv6)
efirtmnet5v6	EFI RTM Network 5 (IPv6)
efirtmnet6v6	EFI RTM Network 6 (IPv6)
efirtmnet7v6	EFI RTM Network 7 (IPv6)
efirtmnet8v6	EFI RTM Network 8 (IPv6)
efirtmnet9v6	EFI RTM Network 9 (IPv6)
efirtmnet10v6	EFI RTM Network 10 (IPv6)

Table 8-15 Boot Order Devices (continued)

Boot Device	Description
efiusb	EFI Boot from USB device
efiusb1	EFI Boot from USB device connected to USB1
efiusb2	EFI Boot from USB device connected to USB2
eifusb3	EFI Boot from USB device connected to USB RTM
windows	Windows Boot Manager
redhat	RedHat Linux
suse	SuSE Linux
ubuntu	Ubuntu Linux
fedora	Fedora Linux

8.1.8 LAN Device Commands

Table 8-16 Supported LAN Device Commands

Command	NetFn (Request/Response)	CMD
Set LAN Configuration Parameters	0x0C/0x0D	0x01
Get LAN Configuration Parameters	0x0C/0x0D	0x02
Set SOL Configuration Parameters	0x0C/0x0D	0x21
Get SOL Configuration Parameters	0x0C/0x0D	0x22

8.2 PICMG 3.0 Commands

The Penguin Edge IPMC is a fully compliant AdvancedTCA intelligent Platform Management Controller. It supports all required and mandatory AdvancedTCA commands as defined in the PICMG 3.0 and AMC.0 R2.0 specifications.

Table 8-17 Supported PICMG 3.0 Commands

Command	NetFn (Request/Response)	CMD	Comments
Get PICMG Properties	0x2C/0x2D	0x00	-
Get Address Info	0x2C/0x2D	0x01	-
FRU Control	0x2C/0x2D	0x04	The blade supports the cold reset and graceful reboot options.
Get FRU LED Properties	0x2C/0x2D	0x05	-
Get FRU LED Color Capabilities	0x2C/0x2D	0x06	-
Set FRU LED State	0x2C/0x2D	0x07	-
Get FRU LED State	0x2C/0x2D	0x08	-
Set IPMB State	0x2C/0x2D	0x09	-
Set FRU Activation Policy	0x2C/0x2D	0x0A	-
Get FRU Activation Policy	0x2C/0x2D	0x0B	-
Set FRU Activation	0x2C/0x2D	0x0C	-
Get Device Locator Record ID	0x2C/0x2D	0x0D	The Penguin Edge IPMCs support the standard PICMG 3.0 and the extended AMC.0 R2.0 versions of this command.
Set Port State	0x2C/0x2D	0x0E	-
Get Port State	0x2C/0x2D	0x0F	-
Compute Power Properties	0x2C/0x2D	0x10	-
Set Power Level	0x2C/0x2D	0x11	-

Table 8-17 Supported PICMG 3.0 Commands (continued)

Command	NetFn (Request/Response)	CMD	Comments
Get Power Level	0x2C/0x2D	0x12	-
Get IPMB Link Info	0x2C/0x2D	0x18	-
Set AMC Port State	0x2C/0x2D	0x19	-
Get AMC Port State	0x2C/0x2D	0x1A	-
Get FRU Control Capabilities	0x2C/0x2D	0x1E	-
Get target upgrade capabilities	0x2C/0x2D	0x2E	-
Get component properties	0x2C/0x2D	0x2F	-
Abort firmware upgrade	0x2C/0x2D	0x30	-
Initiate upgrade action	0x2C/0x2D	0x31	-
Upload firmware block	0x2C/0x2D	0x32	-
Finish firmware upload	0x2C/0x2D	0x33	-
Get upgrade status	0x2C/0x2D	0x34	-
Activate firmware	0x2C/0x2D	0x35	-
Query self-test results	0x2C/0x2D	0x36	-
Query rollback status	0x2C/0x2D	0x37	-
Initiate manual rollback	0x2C/0x2D	0x38	-

The firmware upgrade commands supported by the blade are implemented according to the PICMG HPM.1 Revision 1.0 specification.

The boot block can be updated with PICMG HPM.1 specific commands.

8.3 Penguin Edge Specific Commands

The Penguin Edge IPMC supports several commands which are not defined in the IPMI or PICMG 3.0 specification but are introduced by Penguin Edge: serial output commands.

Before sending any of these commands, the shelf management software must check whether the receiving IPMI controller supports Penguin Edge specific IPMI commands by using the IPMI command, 'Get Device ID'. Sending Penguin Edge specific commands to IPMI controllers which do not support these IPMI commands will lead to no or undefined results.

Proper handling of these commands is required to write a portable application.

8.3.1 Serial Output Commands

Table 8-18 Serial Output Commands

Command Name	NetFn (Request/Response)	CMD	Description
Set Serial Output	0x2E/0x2F	0x15	See *Set Serial Output Command on page 255*
Get Serial Output	0x2E/0x2F	0x16	See *Get Serial Output Command on page 256*

8.3.1.1 Set Serial Output Command

The Set Serial Output command selects the serial port output source for a serial port connector.

8.3.1.1.1 Request Data

The following table lists the request data applicable to the Set Serial Output command.

Table 8-19 Request Data of Set Serial Output Command

Byte	Data Field
1	LSB of Penguin Edge IANA Enterprise number. A value of 0xCD has to be used.
2	Second byte of Penguin Edge IANA Enterprise number. A value of 0x65 has to be used.
3	MSB of Penguin Edge IANA Enterprise number. A value of 0x00 has to be used.

Table 8-19 Request Data of Set Serial Output Command (continued)

Byte	Data Field
4	Serial connector type 0: Face plate connector 1: Backplane connector All other values are reserved. **Note:** Only the face plate connector is supported. No connector on the RTM available.
5	Serial connector instance number. A sequential number that starts from "0".
6	Serial output selector 0: BIOS 2: IPMC debug console All other values are reserved.

8.3.1.1.2 Response Data

The following table lists the response data applicable to the Set Serial Output command.

Table 8-20 Response Data of Set Serial Output Command

Byte	Data Field
1	Completion code
2	LSB of Penguin Edge IANA Enterprise number.
3	Second byte of Penguin Edge IANA Enterprise number.
4	MSB of Penguin Edge IANA Enterprise number.

8.3.1.2 Get Serial Output Command

The Get Serial Output Command provides a way to determine which serial output source goes to a particular serial port connector.

Only BIOS output is supported.

8.3.1.2.1 Request Data

The following table lists the request data applicable to the Get Serial Output command.

Table 8-21 Request Data of Get Serial Output Command

Byte	Data Field
1	LSB of Penguin Edge IANA Enterprise number. A value of 0xCD has to be used.
2	Second byte of Penguin Edge IANA Enterprise number. A value of 0x65 has to be used.
3	MSB of Penguin Edge IANA Enterprise number. A value of 0x00 has to be used.
4	Serial connector type 0: Face plate connector 1: Backplane connector All other values are reserved. **Note**: Only the face plate connector is supported. No connector on the RTM available.
5	Serial connector instance number. A sequential number that starts from 0.

8.3.1.2.2 Response Data

The following table lists the response data applicable to the Get Serial Output command.

Table 8-22 Response Data of Get Serial Output Command

Byte	Data Field
1	Completion code
2	LSB of Penguin Edge IANA Enterprise number.
3	Second byte of Penguin Edge IANA Enterprise number.
4	MSB of Penguin Edge IANA Enterprise number.
5	Serial output selector

8.3.2 OEM Command to configure IPMI Features

Table 8-23 Feature Configuration Command

Command	NetFn (Request/Response)	CMD	Defined in
Set Feature Configuration	0x2E/0x2F	1Eh	*Set Feature Configuration Command on page 259*
Get Feature Configuration	0x2E/0x2F	1Fh	*Get Feature Configuration Command on page 261*

8.3.2.1 Set Feature Configuration

This command can be used to enable/disable features configurations within the IPMC during runtime.

Table 8-24 Set Feature Configuration Command

	Byte	Data Field
Request Data	1	LSB of Penguin Edge IANA Enterprise Number. A value of CDh shall be used.
	2	2nd byte of Penguin Edge IANA Enterprise Number. A value of 65h shall be used.
	3	MSB of Penguin Edge IANA Enterprise Number. A value of 00h shall be used.
	4	Feature Selector. For details, see *Table 8-25*.
	5	Feature Configuration Bit [7-0]: Feature Selector = E0h, E1h 00h = disabled 01h = enabled 02h - 0ffh = reserved Bit [7-0] Feature Selector = 03h: 00h-FFh: Debounce timer timeout value in 100ms
	6	Persistency / Duration 00h = volatile. Actual duration depends on implementation. 01h – FFh = reserved

Table 8-24 Set Feature Configuration Command (continued)

	Byte	Data Field
Response Data	1	Completion Code. Generic plus the following command-specific completion codes: 80h = feature selector not supported. 81h = feature configuration not supported 83h = configuration persistency / duration not supported
	2	LSB of Penguin Edge IANA Enterprise Number. A value of CDh shall be used.
	3	2nd byte of Penguin Edge IANA Enterprise Number. A value of 65h shall be used.
	4	MSB of Penguin Edge IANA Enterprise Number. A value of 00h shall be used.

The following table provides the feature set supported with ATCA-7480.

Table 8-25 Feature Selector Assignments

Feature Selector	Description
(3) 03h	Handle Debounce
(224) E0h	FAILSAFE Function Enable/Disable. For details, see *Fail Safe Logic on page 316*.
(225) E1h	FAIL PROTECT Function Enable/Disable. For details, see *Fail Protect Logic on page 319*.

8.3.2.2 Get Feature Configuration

This command can be used to get the state of feature configuration during IPMC runtime.

Table 8-26 Get Feature Configuration Command

	Byte	Data Field
Request Data	1	LSB of Penguin Edge IANA Enterprise Number. A value of CDh shall be used.
	2	2nd byte of Penguin Edge IANA Enterprise Number. A value of 65h shall be used.
	3	MSB of Penguin Edge IANA Enterprise Number. A value of 00h shall be used.
	4	Feature Selector
Response Data	1	Completion Code. Generic plus the following command-specific completion codes: 80h = feature selector not supported.
	2	LSB of Penguin Edge IANA Enterprise Number. A value of CDh shall be used.
	3	2nd byte of Penguin Edge IANA Enterprise Number. A value of 65h shall be used.
	4	MSB of Penguin Edge IANA Enterprise Number. A value of 00h shall be used.
	5	Feature Configuration. Bit [7-0]: Feature Selector = E0h, E1h 00h = disabled 01h = enabled 02h - 0ffh = reserved Bit [7-0]: Feature Selector = 03h 00h-FFh: Debounce timer timeout value in 100 ms
	6	Persistency / Duration

8.4 Pigeon Point Specific Commands

The IPMC supports additional IPMI commands that are specific to Pigeon Point. This section provides detailed description of those extensions:

Table 8-27 Pigeon Point Extension Commands

Command	NetFn (Request/Response)	CMD
Get Status *Table 8-29 on page 263*	0x2E/0x2F	0x00
Get Serial Interface Properties *Table 8-30 on page 265*	0x2E/0x2F	0x01
Set Serial Interface Properties *Table 8-31 on page 267*	0x2E/0x2F	0x02
Get Debug Level *Table 8-32 on page 268*	0x2E/0x2F	0x03
Set Debug Level *Table 8-33 on page 269*	0x2E/0x2F	0x04
Get Hardware Address *Table 8-34 on page 270*	0x2E/0x2F	0x05
Set Hardware Address *Table 8-35 on page 270*	0x2E/0x2F	0x06
Get Handle Switch *Table 8-36 on page 271*	0x2E/0x2F	0x07
Set Handle Switch *Table 8-37 on page 271*	0x2E/0x2F	0x08
Get Payload Communication Time-Out *Table 8-38 on page 272*	0x2E/0x2F	0x09
Set Payload Communication Time-Out *Table 8-39 on page 273*	0x2E/0x2F	0x0A
Enable Payload Control *Table 8-40 on page 273*	0x2E/0x2F	0x0B
Disable Payload Control *Table 8-41 on page 274*	0x2E/0x2F	0x0C
Reset IPMC *Table 8-42 on page 274*	0x2E/0x2F	0x0D
Hang IPMC *Table 8-43 on page 275*	0x2E/0x2F	0x0E
Graceful Reset *Table 8-44 on page 276*	0x2E/0x2F	0x11
Get Payload Shutdown Time-Out *Table 8-45 on page 276*	0x2E/0x2F	0x15
Set Payload Shutdown Time-Out *Table 8-46 on page 277*	0x2E/0x2F	0x16
Get Module State *Table 8-47 on page 278*	0x2E/0x2F	0x27

Table 8-27 Pigeon Point Extension Commands (continued)

Command	NetFn (Request/Response)	CMD
Enable Module Site *Table 8-48 on page 279*	0x2E/0x2F	0x28
Disable Module Site *Table 8-49 on page 279*	0x2E/0x2F	0x29
Reset Carrier SDR repository *Table 8-50 on page 280*	0x2E/0x2F	0x33

Some of the following commands refer to IPMC modes.

Table 8-28 IPMC Modes

Mode	Description
Standalone	In standalone mode, the carrier IPMC disconnects from IPMB-0 but keeps on listening to the serial debug and payload interfaces and serving requests coming from them, as well as managing the modules, AMC point-to-point (P2P) and clock E-keying. Standalone mode is intended for debugging purposes and/or operation in a non-ATCA environment. In standalone mode, the carrier IPMC automatically activates and deactivates the on-carrier payload and modules whenever it does not violate any carrier limitations.
Manual standalone	Manual standalone mode is equivalent to standalone mode with only one exception: carrier IPMC control over the on-carrier payload is automatically disabled in manual standalone mode.

8.4.1 Get Status Command

The Get Status command can be used by the payload software to retrieve the status of the IPMC.

Table 8-29 Get Status Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
Response Data	1	Completion Code

Table 8-29 Get Status Command Description (continued)

Type	Byte	Data Field
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00
	5	Bit [7] Graceful Reboot Request If set to 1, indicates that the payload is requested to initiate the graceful reboot sequence. Bit [6] Diagnostic Interrupt Request If set to 1, indicates that a payload diagnostic interrupt request has arrived. Bit [5] Shutdown Alert If set to 1, indicates that the payload is going to be shutdown. Bit [4] Reset Alert If set to 1, indicates that the payload is going to be reset. Bit [3] Sensor Alert If set to 1, indicates that at least one of the IPMC sensors detects a threshold crossing. Bits [2:1] Mode The current IPMC modes are defined as: 0: Normal 1: Standalone, for a description refer to *Table 8-28* 2: Manual Standalone, for a description refer to *Table 8-28* Bit [0] Control If set to 0, the IPMC control over the payload is disabled.
	6	Bits [4:7] Metallic Bus 2 Events These bits indicate pending Metallic Bus 2 requests arrived from the shelf manager 0: Metallic Bus 2 Query 1: Metallic Bus 2 Release 2: Metallic Bus 2 Force 3: Metallic Bus 2 Free Bits [0:3] Metallic Bus 1 Events These bits indicate pending Metallic Bus 1 requests arrived from the shelf manager: 0: Metallic Bus 1 Query 1: Metallic Bus 1 Release 2: Metallic Bus 1 Force 3: Metallic Bus 1 Free

Table 8-29 Get Status Command Description (continued)

Type	Byte	Data Field
	7	Bits [4:7] Clock Bus 2 Events These bits indicate pending Clock Bus 2 requests arrived from the shelf manager 0: Clock Bus 2 Query 1: Clock Bus 2 Release 2: Clock Bus 2 Force 3: Clock Bus 2 Free Bits [0:3] Clock Bus 1 Events These bits indicate pending Clock Bus 1 requests arrived from the shelf manager: 0: Clock Bus 1 Query 1: Clock Bus 1 Release 2: Clock Bus 1 Force 3: Clock Bus 1 Free
	8	Bits [4:7] Reserved Bits [0:3] Clock Bus 3 Events These bits indicate pending Clock Bus 3 requests arrived from the shelf manager 0: Clock Bus 3 Query 1: Clock Bus 3 Release 2: Clock Bus 3 Force 3: Clock Bus 3 Free

8.4.2 Get Serial Interface Properties Command

The Get Serial Interface Properties command is used to get the properties of a particular serial interface.

Table 8-30 Get Serial Interface Properties Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4	Interface ID 0: Serial Debug Interface

Table 8-30 Get Serial Interface Properties Command Description (continued)

Type	Byte	Data Field
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00
	5	Bit [7] Echo On If this bit is set, the IPMC enables echo for the given serial interface. Bits [6:4] Reserved Bits [3:0] Baud Rate ID The baud rate ID defines the interface baud rate as follows: 0: 9600 bps 1: 19200 bps 2: 38400 bps 3: 57600 bps (unsupported) 4: 115200 bps (unsupported)

8.4.3 Set Serial Interface Properties Command

The Set Serial Interface Properties command is used to set the properties of a particular serial interface.

Table 8-31 Set Serial Interface Properties Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4	Interface ID 0: Serial Debug Interface
	5	Bit [7] Echo On If this bit is set, the IPMC enables echo for the given serial interface. Bits [6:4] Reserved Bits [3:0] Baud Rate ID The baud rate ID defines the interface baud rate as follows: 0: 9600 bps 1: 19200 bps 2: 38400 bps 3: 57600 bps (unsupported) 4: 115200 bps (unsupported)
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

8.4.4 Get Debug Level Command

The Get Debug Level command gets the current debug level of the IPMC firmware.

Table 8-32 Get Debug Level Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00
	5	Bit [7] IPMB-L Dump Enable If set to "1", the IPMC provides a trace of IPMB-L messages that are arriving to/going from the IPMC via IPMB-L. Bit [6] n/a Bit [5] KCS Dump Enable If set to "1", the IPMC provides a trace of KCS messages that are arriving to/going from the IPMC via KCS. Bit [4] IPMB Dump Enable If set to "1", the IPMC provides a trace of IPMB messages that are arriving to/going from the IPMC via IPMB-O. Bit [3] n/a Bit [2] Alert Logging Enable If set to "1", the IPMC outputs important alert messages onto the serial debug interface. Bit [1] Low-level Error Logging Enable If set to "1", the IPMC outputs low-level error/diagnostic messages onto the serial debug interface. Bit [0] Error Logging Enable If set to "1", the IPMC outputs error/diagnostic messages onto the serial debug interface.

8.4.5 Set Debug Level Command

The Set Debug Level command sets the current debug level of the IPMC firmware.

Table 8-33 Set Debug Level Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4	Bit [7] IPMB-L Dump Enable If set to "1", the IPMC provides a trace of IPMB-L messages that are arriving to/going from the IPMC via IPMB-L. Bit [6] n/a Bit [5] KCS Dump Enable If set to "1", the IPMC provides a trace of KCS messages that are arriving to/going from the IPMC via KCS. Bit [4] IPMB Dump Enable If set to "1", the IPMC provides a trace of IPMB messages that are arriving to/going from the IPMC via IPMB-O. Bit [3] n/a Bit [2] Alert Logging Enable If set to "1", the IPMC outputs important alert messages onto the serial debug interface. Bit [1] Low-level Error Logging Enable If set to "1", the IPMC outputs low-level error/diagnostic messages onto the serial debug interface. Bit [0] Error Logging Enable If set to "1", the IPMC outputs error/diagnostic messages onto the serial debug interface.
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

8.4.6 Get Hardware Address Command

The Get Hardware Address command reads the hardware address of the IPMC.

Table 8-34 Get Hardware Address Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00
	5	Hardware Address

8.4.7 Set Hardware Address Command

The Set Hardware Address command allows to override the hardware address read from hardware when the IPMC operates in (manual) standalone mode (for a description refer to *Table 8-28*).

Table 8-35 Set Hardware Address Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4	Hardware Address If set to 00, the ability to override the hardware address is disabled. Note: A hardware address change only takes effect after an IPMC reset.
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

8.4.8 Get Handle Switch Command

The Get Handle Switch command reads the state of the hot-swap handle of the IPMC. Overriding of the handle switch state is allowed only if the IPMC operates in manual standalone mode (for a description refer to *Table 8-28*).

Table 8-36 Get Handle Switch Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00
	5	Handle Switch Status 0x00: The handle switch is open. 0x01: The handle switch is closed. 0x02: The handle switch state is read from hardware.

8.4.9 Set Handle Switch Command

The Set Handle Switch command sets the state of the hot-swap handle switch in manual standalone mode (for more details, refer to *Table 8-28*).

Table 8-37 Set Handle Switch Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4	Handle Switch Status 0x00: The handle switch is open. 0x01: The handle switch is closed. 0x02: The handle switch state is read from hardware.

Table 8-37 Set Handle Switch Command Description (continued)

Type	Byte	Data Field
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

8.4.10 Get Payload Communication Time-Out Command

The Get Payload Communication Time-Out command reads the payload communication time-out value.

Table 8-38 Get Payload Communication Time-Out Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00
	5	Payload Time-out Payload communication time-out measured in hundreds of milliseconds. Thus, the payload communication time-out may vary from 0.1 to 25.5 seconds.

8.4.11 Set Payload Communication Time-Out Command

The Set Payload Communication Time-Out command sets the payload communication time-out value.

Table 8-39 Set Payload Communication Time-Out Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4	Payload Time-out Payload communication time-out measured in hundreds of milliseconds. Thus, the payload communication time-out may vary from 0.1 to 25.5 seconds.
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

8.4.12 Enable Payload Control Command

The Enable Payload Control command enables payload control from the serial debug interface.

Table 8-40 Enable Payload Control Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

8.4.13 Disable Payload Control Command

The Disable Payload Control command disables payload control from the serial debug interface.

Table 8-41 Disable Payload Control Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

8.4.14 Reset IPMC Command

The Reset IPMC command allows the payload to reset the IPMC over the KCS host interface.

Table 8-42 Reset IPMC Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4	Reset Type Code 0x00: Cold IPMC reset to the Current mode 0x01: Cold IPMC reset to the Normal mode 0x02: Cold IPMC reset to the Standalone mode, for a description refer to *Table 8-28* 0x03: Cold IPMC reset to the Manual Standalone mode, for a description refer to *Table 8-28* 0x04: Reset the IPMC and enter Upgrade mode

Table 8-42 Reset IPMC Command Description (continued)

Type	Byte	Data Field
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

8.4.15 Hang IPMC Command

The IPMC provides a way to test the watchdog timer support by implementing the Hang IPMC command, which simulates firmware hanging by entering an endless loop.

Table 8-43 Hang IPMC Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

8.4.16 Graceful Reset Command

The IPMC supports the Graceful Reboot option of the FRU Control command. On receiving such a command, the IPMC sets the Graceful Reboot Request bit of the IPMC status, sends a status update notification to the payload, and waits for the Graceful Reset command from the payload. If the IPMC receives such a command before the payload communication time-out time, it sends the 0x00 completion code (Success) to the shelf manager. Otherwise, the 0xCC completion code is sent.

The IPMC does not reset the payload upon receiving the Graceful Reset command or time-out. If the IPMC participation is necessary, the payload must request the IPMC to perform a payload reset. The Graceful Reset command is also used to notify the IPMC about the completion of the payload shutdown sequence.

Table 8-44 Graceful Reset Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

8.4.17 Get Payload Shutdown Time-Out Command

When shelf manager commands the IPMC to shut down the payload (that is sends the Activate FRU (Deactivate) command), the IPMC notifies the payload by forwarding the command Activate FRU (Deactivate) to the KCS interface. Provided the OpenIPMI driver has registered this command for notification, the payload gets notified. Upon receiving this notification, the payload software is expected to initiate the payload shutdown sequence. After performing this sequence, the payload should send the Graceful Reset command to the IPMC over the payload Interface to notify the IPMC that the payload shutdown is complete.

To avoid deadlocks that may occur if the payload software does not respond, the IPMC provides a special time-out for the payload shutdown sequence. If the payload does not send the Graceful Reset command within a definite period of time, the IPMC assumes that the payload shutdown sequence is finished, and resets the payload.

Table 8-45 Get Payload Shutdown Time-Out Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00

Table 8-45 Get Payload Shutdown Time-Out Command Description (continued)

Type	Byte	Data Field
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00
	5:6	Time-Out measured in hundreds of milliseconds, LSB first

8.4.18 Set Payload Shutdown Time-Out Command

The Set Payload Shutdown Time-Out command is defined in the following table.

Table 8-46 Set Payload Shutdown Time-Out Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4:5	Time-Out measured in hundreds of milliseconds, LSB first
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

8.4.19 Get Module State Command

The Get Module State command is used to query the state of a module (RTM with site ID1) using any of the external interfaces.

Table 8-47 Get Module State Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4	Module Site ID
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00
	5	Module Status Bit [0] 0: Module site is enabled. 1: Module site is disabled. Bit [1] 0: Module is not present. 1: Module is present. Bit [2] 0: Management power is disabled. 1: Management power is enabled. Bit [3] 0: Management power is bad. 1: Management power is good. Bit [4] 0: Payload power is disabled. 1: Payload power is enabled. Bit [5] 0: Payload power is bad. 1: Payload power is good. Bit [6] 0: IPMB-L buffer is not attached. 1: IPMB-L buffer is attached. Bit [7] 0: IPMB-L buffer is not ready. 1: IPMB-L buffer is ready.

8.4.20 Enable Module Site Command

The Enable Module Site command is used to enable a module site.

Table 8-48 Enable Module Site Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4	Module Site ID
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00

8.4.21 Disable Module Site Command

The Disable Module Site command is used to disable a module site. If a module site is disabled, the IPMC firmware ignores the module inserted and acts as if the module is not present.

Table 8-49 Disable Module Site Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4	Module Site ID
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

8.4.22 Reset Carrier SDR Repository Command

The Reset Carrier SDR Repository command is used to clear and rebuild the carrier SDR repository.

Table 8-50 Reset Carrier SDR Repository Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

IPMI Feature Set

9.1 Overview

The ATCA-7480 provides an intelligent hardware management system, as defined in the AdvancedTCA® Base Specification (PICMG® 3.0; AMC.0). This system incorporates two IPMI controllers:

- An Intelligent Platform Management Controller (IPMC) based on the BMR-A2F-AMCc® reference design from Pigeon Point Systems.
- A Module Management Controller (MMC) residing at the RTM, based on the BMR-AVR-AMCm® reference design from Pigeon Point Systems.

Pigeon Point Systems IPM Sentry products are consistent with all current PICMG specifications as well as IPMI v2.0 compliant.

The ATCA-7480 implements all standard Intelligent Platform Management Interface (IPMI) commands and provides hardware interfaces for other system management features such as Hot Swap control, LED control, power control, as well as temperature and voltage monitoring. The IPMC also supports a Keyboard Controller Style (KCS) based host interface for direct payload to IPMI communication.

The ATCA-7480 provides a rich feature set:

- Carrier SDR Repository
- FRU inventory
- Sensor Management (BIOS/FPGA Boot Bank Sensor, OS Boot Sensor, Boot Error Sensor, Memory Sensor, Firmware Progress Sensor, Reset Cause Sensor, PIM Power Entry specific Sensors, CPU/DIMM temperature sensors, Boot Initiated Sensor, Critical IRQ Sensor, Battery Sensor, CPLD Power Failure Sensors).
- Asynchronous event notification
- RTM hot swap management
- Configurable Ejector Handle Debounce
- HPM.1 firmware upgrades for IPMI, BIOS, and FPGA
- HPM.2 and HPM.3
- BIOS and FPGA Boot Bank supervision
- BIOS Boot Configuration via IPMI
- BIOS Failsafe
- Serial/IPMI over LAN
- Serial Line Selection
- Local System Event Log

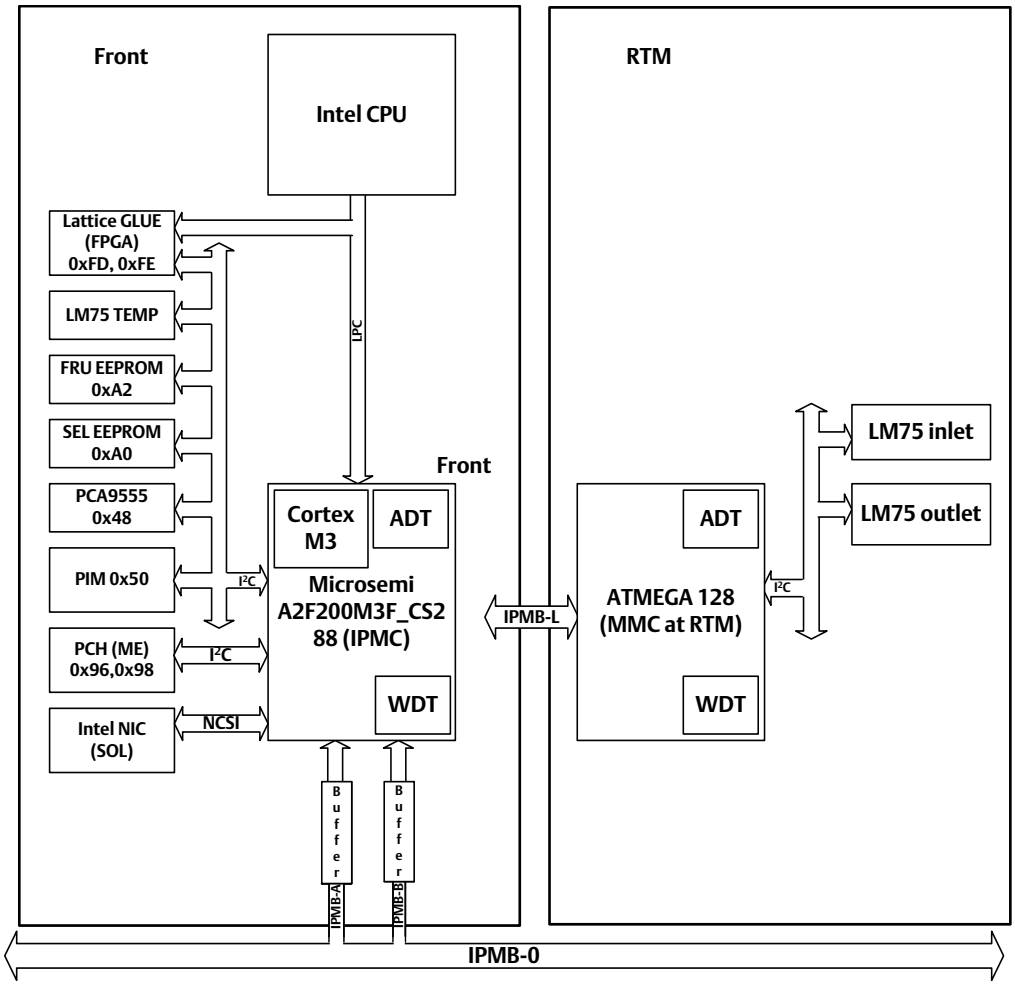
The IPMC at the front board acts like an IPMC carrier. It retrieves the sensor information of the MMC and creates a Sensor Data Record (SDR) repository providing direct access to all sensors within the system. The IPMC is implemented as the managed FRU #0 and the MMC as managed FRU #1. All commands directed to the MMC will be bridged by the IPMC.

The Intel CPU communicates with the IPMC using the KCS interface of the IPMC. The FRU inventory, System Event Log (SEL) events, and the SDR information are stored in external I^2C EEPROMs. This enables post-mortem analysis when the system processor becomes disabled.

Registers within the Glue Logic FPGA can be accessed by the IPMC via I^2C bus. This enhances the capabilities of the IPMC. The Glue Logic FPGA is used to monitor the CPU status, the payload reset cause, the power failure registers, and to control the BIOS boot bank selection.

A functional block diagram of the ATCA-7480 IPMC/MMC system is shown below.

Figure 9-1 IPMC Block Diagram of ATCA-7480



9.2 Firmware Architecture

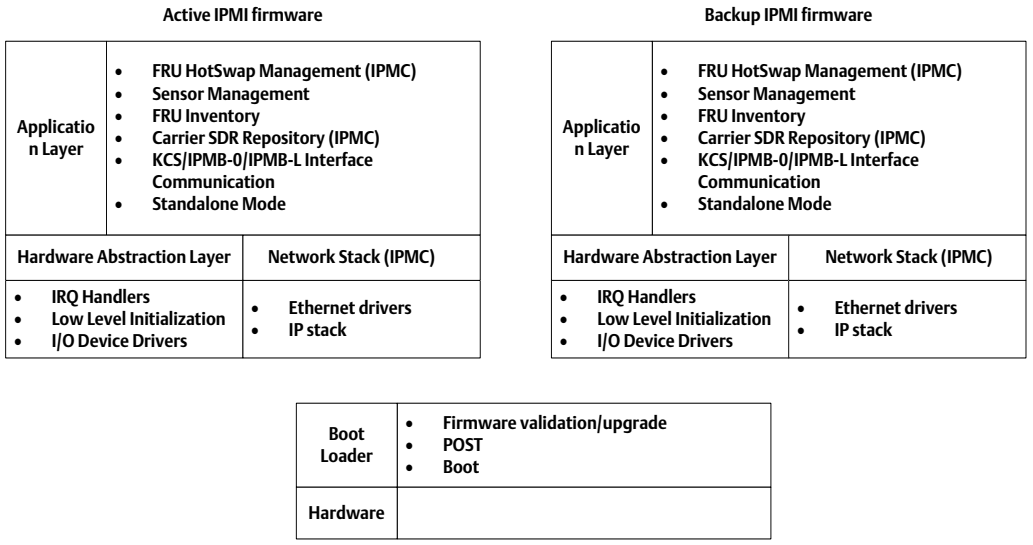
The IPMC and MMC firmware basically consists of four major parts:

- **Boot loader**
  The boot loader maintains redundant copies of the firmware in flash. Each time the IPMI firmware is upgraded, a redundant copy of the current IPMI firmware is made in flash.

- **Hardware Abstraction Layer (HAL)**
  The Hardware Abstraction Layer (HAL) is responsible for initializing the A2F/ATMEL and making all preparations necessary for running the code written in C language. The time management facility of the HAL is responsible for providing a means for measuring time and detecting timeout conditions. The device drivers are responsible for implementing high-level interfaces to the hardware.
- **Network Stack**
  The Network Stack is provided to implement RMCP+ protocols for IPMI-over-LAN and Serial-over-LAN.
- **Application Layer**
  The Application layer is implemented as a multi-threaded application. The main thread reads incoming messages/events from various inbound queues, processes these messages/events, and produces outgoing traffic to appropriate hardware interfaces.
  The IPMC provides a number of subsidiary threads to serve RTM module discovery and e-keying management.
  The Application layer can also operate in standalone mode intended to debug the payload without requiring a shelf manager.

The following figure illustrates the firmware architecture.

Figure 9-2 Firmware Architecture



9.3 Firmware Upgrade

9.3.1 HPM.1 Components

All embedded software images can be upgraded via HPM.1 protocol.

- IPMI bootloader
- IPMI firmware
- IPMI FRU information
- IAP
- BIOS
- FPGA

The above listed items have different component properties due to the different physical implementation.

Table 9-1 HPM.1 components

	ID	Payload cold reset required	Deferred activation support	Comparison support	Preparation support	Rollback/ backup support	Component name
IPMI bootloader	1	no	no	yes	yes	no	IPMC B/L
IPMI firmware	0	yes	yes	yes	yes	supported without backup command	IPMC F/W
FRU information	2	yes	no	yes	yes	supported without backup command	IPMC F/I
IAP	3	no	no	yes	yes	no	IPMC IAP
BIOS	5	yes	no	no	yes	supported without backup command	PYLD F/W
FPGA	4	yes (even power cycle)	no	no	yes	supported without backup command	PYLD FPGA

9.3.1.1 IPMI Boot-loader and Firmware Component

The IPMI firmware stores its active and backup image within one external SPI flash. A small boot loader residing in internal Embedded Non-Volatile Memory (eNVM), is used to copy either the active or the backup image from the external SPI flash into the internal eNVM, depending on the boot flags indicating successful boot. The boot loader is also used as HPM.1 component; however there is no backup image.

The boot loader maintains redundant copies of the firmware in flash. Each time the IPMI firmware is upgraded, a redundant copy of the current IPMI firmware is made in flash. Once the new IPMI firmware is programmed, the IPMI controller will reset itself to boot from the new image. Also, the boot loader validates new IPMI firmware images. The provided IPMI controller can power up successfully and the actual image is made active and the previously active image is made backup. In case power-up fails, the boot loader will automatically recover from crisis and boots from the image.

The IPMI controller can be upgraded via KCS, LAN, or IPMB interface. To ensure that the payload is not interrupted during IPMI firmware upgrade, the IPMI controller stores all operational information (e-keying, hot-swap state, last events to be queued, graceful shutdown timeout, latest pin settings and so on) in non-volatile storage.

9.3.1.2 IAP Component

The BMR-A2F-AMCc IPMI building block from Pigeon Point is implemented within an FPGA logic block from Microsemi Inc. Its fabric can be upgraded via HPM.1 firmware upgrade. This process is referred to In Application Programming (IAP) upgrade.

As there is no possibility of crisis recovery, Penguin Solutions does not recommend to upgrade this component without any need.

9.3.1.3 FPGA Component

The Lattice Glue Logic FPGA is equipped with two SPI flashes; one is called "Active", the other one is "Backup".

During power-up, the IPMC protects the "Active" SPI flash by de-selecting it, once the FPGA boots successfully. Thus, HPM.1 specific logic updates can be performed only to the "Backup" SPI flash. By explicitly prohibiting FPGA logic updates to the "Active" SPI flash, crisis recovery is guaranteed always. Both FPGA flashes cannot be overwritten wrongly even by accidentally.

The information about which FPGA flash is active, is provided using the Boot Bank Supervision Sensor. For more details, see *Boot Bank Supervision Sensor on page 306*.

Besides HPM.1 manual rollback, there is also a possibility to switch the banks without upgrading an HPM.1 firmware at all. For details see *System Boot Options Commands on page 235*.

The HPM.1 command, `Activate Firmware` does not reboot the payload firmware unconditionally. Instead the blade can be power-cycled gracefully to activate the new firmware.

NOTICE

A payload cold reset is not enough to execute a new FPGA component. In this particular case a power cycle is required.

9.3.1.4 BIOS Component

The ATCA-7480 provides two SPI flashes for storing two redundant BIOS firmware images; one is called "Active", the other one is "Backup". Due to the fact that the "Active" SPI flash is routed to the Intel CPU always, the IPMC can perform HPM.1 specific firmware upgrades only to the "Backup" SPI flash.

The information about which BIOS flash is actually active, is provided using the Boot Bank Supervision Sensor. For details, see *Boot Bank Supervision Sensor on page 306*. Besides HPM.1 manual rollback, there is also a possibility to switch the banks without upgrading an HPM.1 firmware at all. For details, see *System Boot Options Commands on page 235*.

Automatic rollback is implemented via failsafe architecture. For details, see *Fail Safe Logic on page 316*.

The HPM.1 command, `Activate Firmware` does not reboot the payload firmware unconditionally. Instead the blade can be rebooted gracefully to activate the firmware.

Crisis recovery is supported fully (two broken SPI flashes can be reprogrammed via IPMI with the help of the ShMM).

9.3.2 Retrieving Versioning Information

Retrieving the actual and backup version of the components is possible without switching payload firmware boot banks (Penguin Solutions strongly recommends to use fcu for embedded firmware upgrades). The following terminal output illustrates the component versions as an example:

```
hayabusa(avh012):119 ./fcu -q -t8a --lan=192.168.42.50
********************[[[[[REPORT BEGIN]]]]]********************
OPERATION : Query
RESULT    : SUCCESS
MESSAGE   : Device              : 0065CD-2003-hpm.1-ipmc
Part number         : 123456789123456789123
Part revision       :
```

```
BANK                : A - Operational
Firmware Name       : IPMI F/W
Firmware Version    : 2.0.00000002


BANK                : B - Rollback
Firmware Name       : IPMI F/W
Firmware Version    : 2.0.00000002


BANK                : D - Operational
Firmware Name       : IPMI B/L
Firmware Version    : 2.0.00000002


BANK                : G - Operational
Firmware Name       : IPMI F/I
Firmware Version    : 0.0.00000000


BANK                : J - Operational
Firmware Name       : PYLD FPGA
Firmware Version    : 0.40.0000000F


BANK                : K - Rollback
Firmware Name       : PYLD FPGA
Firmware Version    : 0.120.00000010


BANK                : M - Operational
Firmware Name       : PYLD F/W
Firmware Version    : 1.0.00000001


BANK                : N - Rollback
Firmware Name       : PYLD F/W
Firmware Version    : 1.0.0000000A

********************[[[[[ REPORT END ]]]]]********************
```

9.3.3 Firmware Upgrade Tool

The primary update mechanism for the ATCA-7480 blade is the FCU tool, which is delivered with the BBS package for the blade. However, the ATCA-7480 blade family also supports upgrades with the ipmitool. Penguin Solutions recommends to use the Pigeon Point System modified Ipmitool 1.8.13-pps2 or later versions.

9.3.3.1 Installing ipmitool

In case of `ipmitool 1.8.13-pps2` is already installed with your BBS package, the following installation is not needed anymore.

Procedure

1. Get the Pigeon Point System ipmitool from the package (ipmitool-1.8.13-pps-2.tgz).
2. Extract the ipmitool-1.8.13-pps-2.tgz file.
   ```
   prompt>tar -xzvf ipmitool-1.8.13-pps-2.tgz
   ```
3. Go to the directory where ipmitool is extracted.
   ```
   prompt>cd <path>/Ipmitool-1.8.13-pps-2
   ```
4. Build the ipmitool.
   ```
   prompt>./configure && make && make install
   ```

9.3.3.2 Updating ipmitool

The ipmitool HPM update requires two steps for an update.

Procedure

1. Upgrade the component.
   ```
   prompt->ipmitool hpm upgrade <file>
   ```
2. Activate the component.
   ```
   prompt-> ipmitool hpm activate
   ```

9.3.3.3 Upgrading Interfaces

The HPM.1 upgrade supports three different interfaces for upgrading the firmware. These are KCS, IPMB-0, and LAN over BASE. The LAN interface is fully supported even if the payload is not powered on (M4). The BASE Ethernet controller is powered with management power.

9.3.3.3.1 KCS

The standard way to upgrade the firmware of the payload is through the KCS interface. The images and the ipmitool need to be on the payload to upgrade.

Example:

```
prompt>ipmitool hpm upgrade <file>
```

9.3.3.3.2 IPMB-0

This interface represents the backplane IPMI bus and allows remote firmware upgrade. The count of the simultaneous upgrades is limited because of the bus speed.

Examples:

- From shelf manager:
  ```
  prompt>ipmitool -t 0x92 hpm upgrade <file>
  ```
- with RMCP:
  ```
  prompt>ipmitool -I lan -H 192.168.34.8 -U Administrator -P
  Administrator -t 0x92 hpm upgrade <file>
  ```

9.3.3.3.3 IPMI over LAN (BASE)

The IPMI over LAN interface uses the BASE Ethernet controller to do firmware upgrades. The interface has to be configured before the first use. Configuring this interface is described in *Configuring SOL Parameters on page 226*.

Example (with RMCP+):

```
prompt->ipmitool -C 1 -I lanplus -U rmcp -P rmcp -H 172.16.0.221 -k gkey
hpm upgrade /root/bios.hpm activate
```

9.3.4 HPM.2 Specific Firmware Updates

To improve the time for firmware upgrades, the IPMC is complaint to the HPM.2 specification and supports large IPMI messages over LAN interfaces (via base interface and from payload host). Thus, firmware upgrades can be executed much faster. This is especially useful with BIOS firmware upgrades when 16 Mbytes of data need to be transferred via IPMI.

Make sure that your firmware upgrade tool (fcu, ipmitool) need to support large IPMI messages over LAN as well.

The following example is provided to enable users to upgrade their firmware very fast from the payload host (one BIOS SPI flash can be upgraded in ~3 minutes).

1. Evaluate IP address of IPMC.

```
root@ATCA7480:~# ipmitool lan print 1
Set in Progress         : Set Complete
Auth Type Support       :
Auth Type Enable        : Callback :
                        : User     :
                        : Operator :
                        : Admin    :
                        : OEM      :
IP Address Source       : Static Address
IP Address              : 172.16.0.221
Subnet Mask             : 255.255.0.0
MAC Address             : ec:9e:cd:10:a0:64
Default Gateway IP      : 172.16.0.1
Default Gateway MAC     : 14:14:14:14:14:14
RMCP+ Cipher Suites     : 0,1,2,3
Cipher Suite Priv Max   : Not Available
root@ATCA7480:~#
```

2. Configure base interface into IPMC subnet (instead the IP of the IPMC can be changed as well).

```
root@ATCA7480:~# ./ifconfig base1:1 172.16.0.70
```

3. Upgrade the firmware.

```
root@ATCA7480:~# ./ipmitool -C 1 -I lanplus -U rmcp -P rmcp -H 172.16.0.221
-k gkey hpm upgrade /root/bios.hpm activate
PICMG HPM.1 Upgrade Agent 1.0.9:

Validating firmware image integrity...OK
Performing preparation stage...
Services may be affected during upgrade. Do you wish to continue? y/n y
OK

Performing upgrade stage:

-------------------------------------------------------------------------
-------
|ID  | Name       |                  Versions                     | %  |
|    |            |     Active     |     Backup     |     File      |    |
```

```
|----|-------------|-----------------|-----------------|----------------
-|----|
|*  6|PYLD F/W    | 128.02 00000003 | 128.02 00000003 |   0.02 00000003
|100%|
|   |Upload Time: 01:40           | Image Size: 16777217 bytes            |
--------------------------------------------------------------------------
-------
(*) Component requires Payload Cold Reset
Performing activation stage:

Firmware upgrade procedure successful
```

9.4 Sensors

This section provides a description of all analog and discrete sensors available on the ATCA-7480.

Table 9-2 lists the sensor identification numbers and information regarding the sensor type, name, supported thresholds, assertion and de-assertion information, and a brief description of the sensor purpose.

Table 9-2 ATCA-7480 Specific Sensors

Sensor Number	Sensor Name	Sensor Type	Event/Reading Type	Event Data Byte 1	Event Data Byte 2	Event Data Byte 3	Event Threshold/ Description	Assertion Deassertion	Rearm
0	Hot Swap Carrier	Hot Swap 0xF0	Sensor-specific discrete 0x6F	0x0 0x1 0x2 0x3 0x4 0x5 0x6 0x7	[7:4] = Cause [3:0] = Previous State	FRU ID	0x0: M0 0x1: M1 0x2: M2 0x3: M3 0x4: M4 0x5: M5 0x6: M6 0x7: M7	Asrt	Auto
1	Hot Swap RTM	Hot Swap 0xF0	Sensor-specific discrete 0x6F	0x0 0x1 0x2 0x3 0x4 0x5 0x6 0x7	[7:4] = Cause [3:0] = Previous State	FRU ID	0x0: M0 0x1: M1 0x2: M2 0x3: M3 0x4: M4 0x5: M5 0x6: M6 0x7: M7	Asrt	Auto

Table 9-2 ATCA-7480 Specific Sensors (continued)

Sensor Number	Sensor Name	Sensor Type	Event/Reading Type	Event Data Byte 1	Event Data Byte 2	Event Data Byte 3	Event Threshold/ Description	Assertion Deassertion	Rearm
2	IPMB Physical	Physical IPMB-0 0xF1	Sensor-specific discrete 0x6F	0x0 0x1 0x2 0x3	[7:4] = Channel Number [3:0] = Reserved	reading	0x0: IPMB-A disabled, IPMB-B disabled 0x1: IPMB-A enabled, IPMB-B disabled 0x2: IPMB-A disabled, IPMB-B enabled 0x3: IPMB-A enabled, IPMB-B enabled	Asrt	Auto

Table 9-2 ATCA-7480 Specific Sensors (continued)

Sensor Number	Sensor Name	Sensor Type	Event/Reading Type	Event Data Byte 1	Event Data Byte 2	Event Data Byte 3	Event Threshold/ Description	Assertion Deassertion	Rearm
3	Version change	Version Change 0x2B	Sensor-specific discrete 0x6F	0x0 0x1 0x2 0x3 0x4 0x5 0x6 0x7	Change type	0xFF	0x0: Hardware change 0x1: Firmware or software change 0x2: Hardware incompatibility 0x3: Firmware or software incompatibility 0x4: Entity is of an invalid hardware version 0x5: Entity contains invalid F/W,software 0x6: Hardware Change successful 0x7: Software or F/W change successful	Asrt	Auto
4	Mid air temp	Temp 0x01	Threshold 0x01		reading	threshold	unr uc unc	Asrt / Deass	Auto
5	+3.3V MGMT	Voltage 0x02	Threshold 0x01		reading	threshold	unr uc lnr lc	Asrt / Deass	Auto
6	+12V	Voltage 0x02	Threshold 0x01		reading	threshold	unr uc lnr lc	Asrt / Deass	Auto

Table 9-2 ATCA-7480 Specific Sensors (continued)

Sensor Number	Sensor Name	Sensor Type	Event/Reading Type	Event Data Byte 1	Event Data Byte 2	Event Data Byte 3	Event Threshold/ Description	Assertion Deassertion	Rearm
7	+5V	Voltage 0x02	Threshold 0x01		reading	threshold	unr uc lnr lc	Asrt / Deass	Auto
8	RTM 3.3 MGMT	Voltage 0x02	Threshold 0x01		reading	threshold	unr uc lnr lc	Asrt / Deass	Auto
9	RTM 12V	Voltage 0x02	Threshold 0x01		reading	threshold	unr uc lnr lc	Asrt / Deass	Auto
10	Inlet Temp	Temp 0x01	Threshold 0x01		reading	threshold	unr uc unc	Asrt / Deass	Auto
11	Outlet Temp	Temp 0x01	Threshold 0x01		reading	threshold	unr uc unc	Asrt / Deass	Auto
12	BMC Watchdog	Watchdog 2 0x23	Sensor-specific discrete 0x6F	0x0 0x1 0x2 0x3 0x8	See IPMI Spec	0xFF	0x0: Timer expired 0x1: Hard Reset 0x2: Power Down 0x3: Power Cycle 0x8: Timer Interrupt	Asrt	Auto
13	Fw Progress	System Firmware Progress 0x0F	Sensor-specific discrete 0x6F	0x0 0x1 0x2	See IPMI Spec	See *BIOS Supported IPMI Events on page 214*.	0x0: System Firmware Error 0x1: System Firmware Hang 0x2: System Firmware Progress	Asrt	Auto

Table 9-2 ATCA-7480 Specific Sensors (continued)

Sensor Number	Sensor Name	Sensor Type	Event/Reading Type	Event Data Byte 1	Event Data Byte 2	Event Data Byte 3	Event Threshold/ Description	Assertion Deassertion	Rearm
14	OS Boot	OS Boot 0x1F	Sensor-specific discrete 0x6F	0x0 0x1 0x2 0x3 0x4 0x5 0x6	0xFF	0xFF	0x0: A: boot completed 0x1: C: boot completed 0x2: PXE boot completed 0x3: Diagnostic boot completed 0x4: CD_ROM boot completed 0x5: ROM boot completed 0x6: boot completed	Asrt	Auto
15	Boot Error	Boot Error 0x1E	Sensor-specific discrete 0x6F	0x0	0xFF	0xFF	0x0: No Bootable media	Asrt	Auto
16	Boot Initiated	System Boot Initiated 0x1D	Sensor-specific discrete 0x6F	0x0 0x1	0xFF	0xFF	0x0: Initiated by power up 0x1: Initiated by hard reset	Asrt	Auto

Table 9-2 ATCA-7480 Specific Sensors (continued)

Sensor Number	Sensor Name	Sensor Type	Event/Reading Type	Event Data Byte 1	Event Data Byte 2	Event Data Byte 3	Event Threshold/ Description	Assertion Deassertion	Rearm
17	Memory	Memory 0x0C	Sensor-specific discrete 0x6F	0x0 0x1 0x4 0x5 0x6 0x7	0xFF	DIMM identification See *BIOS Supported IPMI Events on page 214*.	0x0: Correctable ECC 0x1: Uncorrectable ECC 0x4: Memory Device Disabled 0x5: Correctable ECC 0x6: Presence detected 0x7: Configuration error.	Asrt	Auto
18	Critical IRQ	Critical Interrupt 0x13	Sensor-specific discrete 0x6F	0x4 0x5	Bus Number See *BIOS Supported IPMI Events on page 214*.	Function/ Device See *BIOS Supported IPMI Events on page 214*.	0x4: PCI PERR 0x5: PCI SERR	Asrt	Auto
19	Battery	Battery 0x29	Sensor-specific discrete 0x6F	0x1	0xFF	0xFF	0x1: Battery failed	Asrt	Auto
20	BootBank	OEM 0xD2	Sensor-specific discrete 0x6F	0x0 0x1	0xFF	0xFF	0x0: Boot Bank A/B 0x1: FPGA Bank A/B	Asrt / Deass	Auto

Table 9-2 ATCA-7480 Specific Sensors (continued)

Sensor Number	Sensor Name	Sensor Type	Event/Reading Type	Event Data Byte 1	Event Data Byte 2	Event Data Byte 3	Event Threshold/ Description	Assertion Deassertion	Rearm
21	ATCA-7480 IPMC	OEM 0xD5	Sensor-specific discrete 0x6F	0x0 0x1 0x2 0x3 0x4 0x5	0xFF	0xFF	0x0: Watchdog Reset 0x1: Software Reset 0x2: Power Failure 0x3: External Reset 0x4: Hard Boot 0x5: Cold Boot		Auto
22	Power Good	Power Supply 0x08	Sensor-specific discrete 0x6F	0x0 0x1	See IPMI Spec	0xFF	0x0: Presence detected 0x1: Power Supply Failure detected	Asrt	Auto
23	-48v A Volts	Voltage 0x02	Threshold 0x01		reading	threshold	unr uc lnr lc	Asrt / Deass	Auto
24	-48v B Volts	Voltage 0x02	Threshold 0x01		reading	threshold	unr uc lnr lc	Asrt / Deass	Auto
25	-48v Amps	Current 0x03	Threshold 0x01		reading	threshold	No Thresholds		Auto
26	HoldUp Cap Volts	Voltage 0x02	Threshold 0x01		reading	threshold	unr uc lnr lc	Asrt / Deass	Auto
27	PWR Entry Temp	Temp 0x01	Threshold 0x01		reading	threshold	unr uc unc	Asrt / Deass	Auto

Table 9-2 ATCA-7480 Specific Sensors (continued)

Sensor Number	Sensor Name	Sensor Type	Event/Reading Type	Event Data Byte 1	Event Data Byte 2	Event Data Byte 3	Event Threshold/ Description	Assertion Deassertion	Rearm
28	PWR Entry Status	OEM 0xD7	Sensor-specific discrete 0x6F	0x0	[6] = VOUT_low [5] = Hotswap [4] = Holdup [2] = Alarm [1] = Enable_B [0] Enable_A	0x0	0x0: Pwr Entry Module Status Change detected	Asrt	Auto
29	48V A Supply	Power Supply 0x08	Sensor-specific discrete 0x6F	0x0 0x1	See IPMI Spec	0xFF	0x0: Presence detected 0x1: Power Supply Failure detected	Asrt / Deass	Auto
30	48V B Supply	Power Supply 0x08	Sensor-specific discrete 0x6F	0x0 0x1	See IPMI Spec	0xFF	0x0: Presence detected 0x1: Power Supply Failure detected	Asrt / Deass	Auto
31	BIOS POST code	OEM 0xD1	Sensor-specific discrete 0x6F	0x0	-	-	0x0: No events for this sensor. Reading according to EFI BIOS port80 status codes.	Asrt	Auto

Table 9-2 ATCA-7480 Specific Sensors (continued)

Sensor Number	Sensor Name	Sensor Type	Event/Reading Type	Event Data Byte 1	Event Data Byte 2	Event Data Byte 3	Event Threshold/ Description	Assertion Deassertion	Rearm
32	Reset Source	OEM 0xDA	Sensor-specific discrete 0x6F	0x0 0x2	[7] = IPMC Payload Reset [6] = PCH Platform Reset [5] = Reserved [4] = Push Button Reset RTM [3] = Reserved [2] = Push Button Reset [1] = XDP Reset [0] = Power GOOD Reset	[1] IPMC Watchdog Pre-Timeout [0] IPMC Watchdog Timeout	0x0: Payload Reset detected. Cause delivered in Event Byte 2/3	Asrt	Auto
33	ACPI State	System ACPI Power State 0x22	Sensor-specific discrete 0x6F	0x0 0x3 0x5	0xFF	0xFF	0x0: S0 0x3: S3 0x5: S5	Asrt	Auto
34	CPU Status	Processor 0x07	Sensor-specific discrete 0x6F	0x0 0x1	0xFF	0xFF	0x0: IERR 0x1: Thermal Trip	Asrt	Auto
35	ME Pwr Fail	OEM 0xE0	Sensor-specific discrete 0x6F	0x0 0x1 0x2 0x7	0xFF	0xFF	0x0: Me Fail State 0x1: Me Fail State 0x2: Me Fail State	Asrt	Auto

Table 9-2 ATCA-7480 Specific Sensors (continued)

Sensor Number	Sensor Name	Sensor Type	Event/Reading Type	Event Data Byte 1	Event Data Byte 2	Event Data Byte 3	Event Threshold/ Description	Assertion Deassertion	Rearm
36	PYLD Pwr Fail S	OEM 0xE1	Sensor-specific discrete 0x6F	0x0 0x1 0x2 0x7	0xFF	0xFF	0x0: Pyld Fail State 0x1: Pyld Fail State 0x2: Pyld Fail State	Asrt	Auto
37	PYLD Pwr Fail C1	OEM 0xE2	Sensor-specific discrete 0x6F	0x0 0x1 0x2 0x7	0xFF	0xFF	0x0: Pyld Wake UP Fail 0x1: VCCIO PG Fail 0x2: Reserved 0x7: Thermtrip	Asrt	Auto
38	PYLD Pwr Fail C2	OEM 0xE3	Sensor-specific discrete 0x6F	0x0 0x1 0x2 0x7	0xFF	0xFF	0x0: 12V PG 0x1: 5V AUX PG 0x2: 5V PG 0x7: 1.5V PG	Asrt	Auto
39	PYLD Pwr Fail C3	OEM 0xE4	Sensor-specific discrete 0x6F	0x0 0x1 0x2 0x7	0xFF	0xFF	0x0: VPP CPU0 PG 0x1: VPP CPU1 PG 0x2: VDD CPU0 PG 0x7: VCCIN CPU1 PG	Asrt	Auto
40	CPU0 temp	Temp 0x01	Threshold 0x01		reading	threshold	unr uc unc	Asrt / Deass	Auto

Table 9-2 ATCA-7480 Specific Sensors (continued)

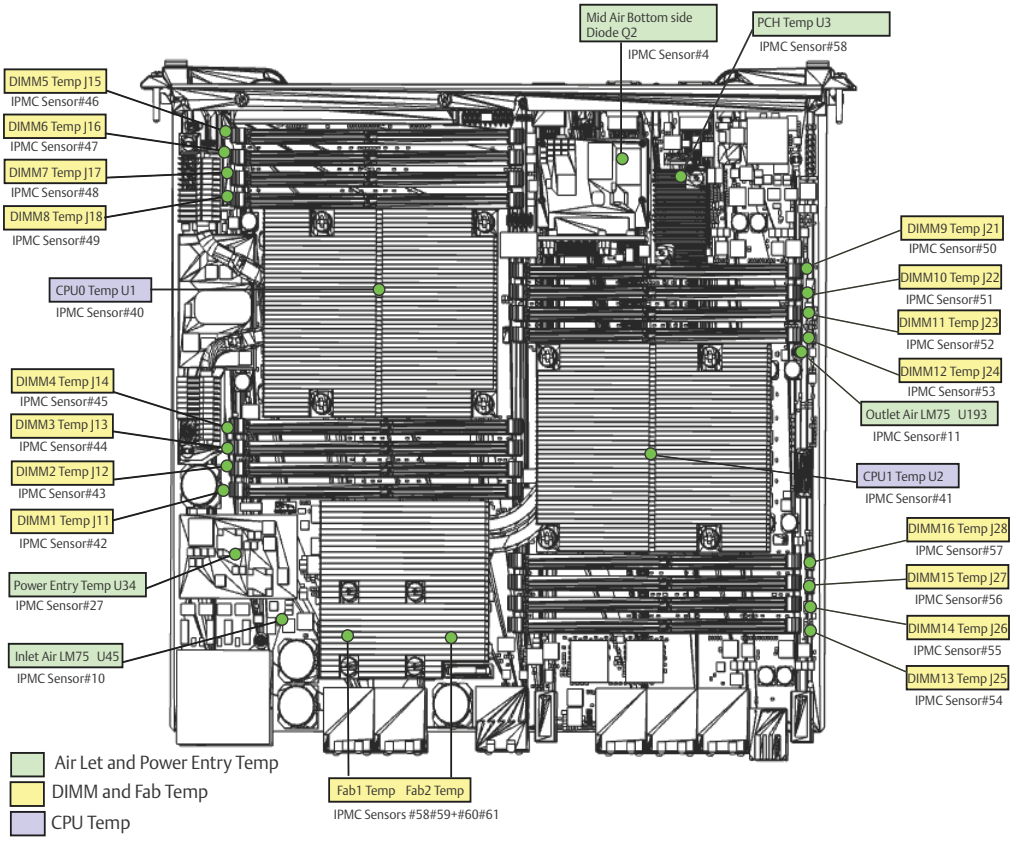
Sensor Number	Sensor Name	Sensor Type	Event/Reading Type	Event Data Byte 1	Event Data Byte 2	Event Data Byte 3	Event Threshold/ Description	Assertion Deassertion	Rearm
41	CPU1 temp	Temp 0x01	Threshold 0x01		reading	threshold	unr uc unc	Asrt / Deass	Auto
42	DDR1 J11 temp	Temp 0x01	Threshold 0x01		reading	threshold	unr uc unc	Asrt / Deass	Auto
43	DDR2 J12 temp	Temp 0x01	Threshold 0x01		reading	threshold	unr uc unc	Asrt / Deass	Auto
44	DDR3 J13 temp	Temp 0x01	Threshold 0x01		reading	threshold	unr uc unc	Asrt / Deass	Auto
45	DDR4 J14 temp	Temp 0x01	Threshold 0x01		reading	threshold	unr uc unc	Asrt / Deass	Auto
46	DDR5 J15 temp	Temp 0x01	Threshold 0x01		reading	threshold	unr uc unc	Asrt / Deass	Auto
47	DDR6 J16 temp	Temp 0x01	Threshold 0x01		reading	threshold	unr uc unc	Asrt / Deass	Auto
48	DDR7 J17 temp	Temp 0x01	Threshold 0x01		reading	threshold	unr uc unc	Asrt / Deass	Auto
49	DDR8 J18 temp	Temp 0x01	Threshold 0x01		reading	threshold	unr uc unc	Asrt / Deass	Auto
50	DDR9 J21 temp	Temp 0x01	Threshold 0x01		reading	threshold	unr uc unc	Asrt / Deass	Auto
51	DDR10 J22 temp	Temp 0x01	Threshold 0x01		reading	threshold	unr uc unc	Asrt / Deass	Auto
52	DDR11 J23 temp	Temp 0x01	Threshold 0x01		reading	threshold	unr uc unc	Asrt / Deass	Auto

Table 9-2 ATCA-7480 Specific Sensors (continued)

Sensor Number	Sensor Name	Sensor Type	Event/Reading Type	Event Data Byte 1	Event Data Byte 2	Event Data Byte 3	Event Threshold/ Description	Assertion Deassertion	Rearm
53	DDR12 J24 temp	Temp 0x01	Threshold 0x01		reading	threshold	unr uc unc	Asrt / Deass	Auto
54	DDR13 J25 temp	Temp 0x01	Threshold 0x01		reading	threshold	unr uc unc	Asrt / Deass	Auto
55	DDR14 J26 temp	Temp 0x01	Threshold 0x01		reading	threshold	unr uc unc	Asrt / Deass	Auto
56	DDR15 J27 temp	Temp 0x01	Threshold 0x01		reading	threshold	unr uc unc	Asrt / Deass	Auto
57	DDR16 J28 temp	Temp 0x01	Threshold 0x01		reading	threshold	unr uc unc	Asrt / Deass	Auto
58	PCH temp	Temp 0x01	Threshold 0x01		reading	threshold	unr uc unc	Asrt / Deass	Auto
59	ADT7461 #L1 temp	Temp 0x01	Threshold 0x01		reading	threshold	unr uc unc	Asrt / Deass	Auto
60	ADT7461 #R1 temp	Temp 0x01	Threshold 0x01		reading	threshold	unr uc unc	Asrt / Deass	Auto
61	ADT7461 #L2 temp	Temp 0x01	Threshold 0x01		reading	threshold	unr uc unc	Asrt / Deass	Auto
62	ADT7461 #R2 temp	Temp 0x01	Threshold 0x01		reading	threshold	unr uc unc	Asrt / Deass	Auto
63	IPMC POST	Management Subsystem Health 0x28	digital Discrete 0x06	0x0 0x1	0xFF	0xFF	0x0: Performance Met 0x1: Performance Lags	Ass	Auto

The following figure shows the locations of all the temperature sensors available on board.

Figure 9-3 Temperature Sensors Location



9.4.1 Payload Driven Sensors

The IPMC firmware provides Firmware Progress, OS Boot, Boot Initiated, Memory, Battery, Critical IRQ and Boot Error sensors to enable payload firmware and payload OS to report boot progress/failure via IPMI event messages.

The firmware progress sensor implemented with sensor type `0x0F` (System Firmware Progress) is used to pass payload boot progress information to the IPMC.

The OS Boot sensor implemented with sensor type `0x1F` (OS Boot) is used to inform the IPMC when the operating system has completed its boot up sequence.

The Boot Initiated sensor implemented with sensor type 0x1D (System Boot Initiated) is used to give additional information about how the boot-up sequence is initiated (by hard reset, by soft reset, and so on).

The Memory sensor implemented with sensor type 0x0C (Memory) is used to inform the IPMC about defect DIMMs detected during power-up.

The Battery sensor implemented with sensor type 0x29 (Battery) is used to inform the IPMC about low/failed RTC.

The Critical IRQ sensor implemented with sensor type 0x13 (Critical Interrupt) is used to give PCI errors and NMIs.

The boot error sensor implemented with sensor type 0x1E (Boot Error) is used to pass boot failure information to the IPMC.

In all cases above, the IPMC sends an event to the ShMM.

9.4.2 Boot Bank Supervision Sensor

The boot bank supervision sensor is intended to always give the actual boot bank from which the payload has booted last.

Table 9-3 Event Data of Boot Bank Sensor

Event Data 1	Event Data 2	Event Data 3
bit[0] 0 = BIOS Bank A; 1 = BIOS Bank B bit[1] 0 = FPGA Bank A; 1 = FPGA Bank B	0xFF	0xFF

The boot bank information received from this sensor may differ from the boot bank selection performed, in case the boot bank selection has changed after the payload has booted. For details, see *BIOS Boot Bank Selection on page 315*.

9.4.3 IPMC POST Results Sensor

The POST results sensor is of type 0x28 (Management subsystem health). It returns information about whether the power-on self-test (POST) of the IPMI firmware passes or not. For more details about the POST, see *POST on page 310*.

9.4.4 Power Good Sensor

The Payload Power sensor is of type 0x08 (Power Supply), which reports the state of the payload power. As the Digital Power Monitor can disable payload power by its own due to a faulty DC-DC converter, the IPMC monitors the health and reports an event in the case where the Digital Power Monitor disables power-on by its own. As a result of this, the IPMC will pro-actively transition the IPMC from M4 to M6 (to M1) with a cause code of 0x09 (Unexpected Deactivation). This automatic shutdown is meant to keep the IPMC's state in-line with the payload state.

9.4.5 Power Interface Sensors

An Ericsson Power input module (PIM4328) is used for the 48V to 12V conversion monitoring. The PIM includes sensors, which monitor the shelf's 48V input feeds current, hold-up capacitor voltage, on-board temperature, and internal status. The status sensor reading can be decoded as shown in the following table.

Table 9-4 Status Sensor's Sensor Reading

Bit 7	Reserved	0
Bit 6	-48V Output Under Voltage Alarm	0: Output Voltage is below threshold 1: Output Voltage is above threshold
Bit 5	Hot-swap Switch State	0: Hot-swap switch is off 1: Hot-swap switch is on
Bit 4	Holdup Switch State	0: Holdup Cap is not connected to -48V Out 1: Holdup Cap is connected to -48V Out
Bit 3	Reserved	0
Bit 2	Alarm Signal State	0: Primary side Alarm is not set 1: Primary side Alarm is set
Bit 1	Voltage Feed B Enabled	0: Enable B is Disabled 1: Enable B is Enabled
Bit 0	Voltage Feed A Enabled	0: Enable A is Disabled 1: Enable A is Enabled

9.4.6 Reset Cause Sensor

This sensor is used to monitor the last payload reset cause (hard reset, front panel reset or any other reset). The IPMC evaluates the Reset Cause Register within the Glue Logic FPGA.

9.4.7 Voltage and Temperature Sensor

There is a selection of voltage and temperature sensors at the front blade and at the RTM.

Table 9-5 Voltage and Temperature Sensor Devices

I^2C Address	I^2C Bus	Domain	Purpose	Device
0x50	IPMC private 2	Front blade	48V Feed A 48V Feed B Current Holdup Temp Status	Power Entry Module
0x90	IPMC private 2	Front blade	Temperature Inlet	LM75
0x94	IPMC private 2	Front blade	Temperature Outlet	LM75
0x2e	IPMC private 4	Front blade	Temperature DIMMs and CPU	ME Engine
Internal ADC		Front blade	Temperature +3.3V Mgmt +12V +1.2V +3.3V +5V RTM 3.3V Mgmt RTM 12V	A2F ADC
0x90	MMC	RTM	Temperature Inlet	LM75
0x92	MMC	RTM	Temperature Outlet	LM75
Internal ADC	MMC	RTM	12V 3.3V 1.05V 0.8V	ATMEL ADC

9.4.8 ME Power Failure Sensor

The IPMC evaluates the ME Power Failure Register to report power failures at the ME engine domain. When a ME failure occurs, the red power failure LED (signal PWR_FAIL_) is blinking.

The error state is kept until ME wakes up (signal SLP_A_ becomes high). For more information, see *Table 5-47*.

For failing states and their coding, see *Table 5-48*.

9.4.9 Payload Power Failure State Sensor

The IPMC evaluates the Payload Power Failure Register to report power failures at the payload domain.

When a Payload Power failure occurs, the red power failure LED is switched ON (signal PWR_FAIL_ is driven low).

The power failing state is maintained until Payload power is turned off.

- Manual Powering: Setting the switch SW100. 1 from OFF to ON.
- IPMC Controlled Powering: The IPMC shutting down the payload power (signal IPMC_VP48_EN_ is deserted). For more information, see *Table 5-50*.

For all possible failing states and their coding, see *Table 5-51*. When the board is powered via switch SW100.1, the debug mode is enabled, where some timeouts are disabled.

9.4.10 Payload Power Failure Cause Sensor

The IPMC uses three sensors to monitor the power failure cause of the payload domain. *Table 5-52* gives more details about the payload power failure. The Payload Power Failure Registers 1 to 3 are always 0 when the Payload Power Failure status (bit 7) is not set.

The Payload Power Failure Cause Register 2 covers the main board voltages. For more information, see *Table 5-52*.

The Payload Power Failure Cause Register 3 covers CPU specific voltages. When a CPU is not mounted (detected via CPU0_SKTOCC_ and CPU1_SKTOCC_) the corresponding power failure bits will never be set. For more information, see *Table 5-54*.

9.5 POST

POST is executed at IPMC startup when either a hard (blade physically extracted/reinserted) or a cold (IPMI Command) reset is performed. POST verifies the functionality of SRAM, IPMB-0, EEPROM data storage, FRU-Information, and all devices (primarily sensors) attached to the IPMC's private master-only I^2C bus. A detailed description of POST tests are as follows:

- **FRU-InformationU** - Verifies that the FRU-Information is readable from the external EEPROM where it is stored. Once read, each section's checksum is computed and validated.
- **IPMB-0U** - Reads the ready signals coming from the I^2C buffers. If this test passes, both ready signals are active and both IPMB busses (IPMB-A and IPMB-B) are enabled.
- **EEPROMU** - Verifies that the EEPROM contents are readable via I^2C. Since the IPMC stores its runtime and persistent data here, proper operation is crucial.
- **Master-Only I^2CU** - Verifies that all expected devices attached to the master-only I^2C bus are accessible.

To obtain results of POST, the IPMC supports the IPMI standard command, `Get Self Test Results` with OEM extensions. This IPMI command can be run at anytime.

9.6 Ejector Handle De-Bounce

The handle switch de-bouncing algorithm is used to configure a programmable delay. The IPMC waits before ejector handle state changes are accepted. This is provided to avoid accidental FRU extraction caused by service-teams during servicing other FRUs.

The ejector handle de-bounce function can be enabled, disabled and configured with the use of the OEM command, `Set/Get Feature Configuration`. For details, see *Set Feature Configuration on page 259*.

9.7 FRU Inventory

The ATCA-7480 implements two intelligent FRUs (IPMC and MMC).

Every FRU provides its own FRU information (serial, part, MAC addresses). Depending on the presence of a module, its FRU information is visible or not.

Table 9-6 FRU information and SEL at EEPROM storage

I²C Address	I²C bus	Domain	Purpose
0xA0	IPMC	Front blade	SEL
0xA2	IPMC	Front blade	FRU Information and Bios Boot Parameter
Device internal	MMC	RTM	FRU Information

The FRU of the RTM is not hot-swappable. This is especially important to ensure that the system management application (HPI-B) does not has to deal with dynamic FRU population.

The MAC addresses of a FRU are stored within the multi-record area of the FRU information. Penguin Edge has defined a MAC address multi-record for this purpose. For details, see *MAC Address FRU OEM Records on page 311*.

9.7.1 MAC Address FRU OEM Records

The MAC Address record is specified in the following table.

Table 9-7 MAC Address Record

Offset	Length	Description
0	1	Record Type ID. A value of C0h (OEM) shall be used for Penguin Edge OEM records.
1	1	End of List/Version [7] End of List. Set to 1b for the last record [6:4] Reserved. Write as 000b. [3:0] Record format version. Write as 2h.
2	1	Record Length
3	1	Record Checksum (zero checksum)
4	1	Header Checksum (zero checksum)
5	1	LSB of Manufacturer ID. Write as CDh.
6	1	Second Byte of Manufacturer ID. Write as 65h.
7	1	MSB of Manufacturer ID. Write as 00h.
8	1	Penguin Edge Record ID. 01h for Penguin Edge MAC Address Record.
9	1	Record Format Version. 01h for this specification.

Table 9-7 MAC Address Record (continued)

Offset	Length	Description
10	1	Number of MAC Address Descriptors (N).
11	N*9	ATCA-7480 MAC Address Descriptors. Refer to XTable 7, MAC Address Descriptor

Table 9-8 MAC Address Descriptor

Offset	Length	Description
0	1	Interface Type. Refer to XTable 8, Interface Type Assignments
1	1	Length Identifier (for example: 6 = 48 bit MAC, 8 = WWPN)
2	1	MAC Address Count (M) (specifying a continuous pool of MAC addresses starting with the MAC address specified in this descriptor) M = 1: this descriptor specifies one MAC address M > 1: this descriptor specifies a pool of MAC addresses with M count
3	6	MAC Address. (Canonical form, the LSB (least significant bit) first.

Table 9-9 Interface Type Assignments

Interface Type	Description
01h	ATCA Base Interface
02h	ATCA Fabric Interface
03h	Front/Rear Panel
04h	Mezzanine Module
05h	Serial over LAN (SOL)
06h	Fibre Channel / WWPN
07h	AMC/MicroTCA Common Options Region
08h	AMC/MicroTCA Fat Pipe Region
09h	AMC/MicroTCA Extended Fat Pipe Region
10h	ATCA Update Channel
11h	Multi-type (Base, Fabric, and Update channel (or two types of it) are connected to a onboard switch)
11h - FFh	reserved

The IPMC provides 10 MAC addresses in its FRU information.

- 4 x 40G fabric implemented with two Fortville NIC
- 2 x 1G Base and 2 x 1G to front implemented with one Powerville NIC
- 2 x SOL

9.8 Reset and Power Domain

The ATCA-7480 provides the following FRU instances:

- FRU #0: front board management and switch
- FRU #1: RTM

Each FRU instance can be reset separately.

9.9 Power Configuration

With respect to the product version, the maximum power consumption requested by the IPMC is different.

Table 9-10 Power Consumption Depending on the Product Version

Item	Value	Description
Dynamic power reconfiguration support	No	While the blade is powered, it supports only one power level.
Dynamic power configuration	No	The power level is fixed and does not change).
Number of power draw levels	1	The amount of possible power levels
Early Power Draw Levels, Watt	-	Complete early power level including IPMC
Steady state Power Draw Levels, Watt	CFG0000/75W CPUs, 16 DIMMs) - 275 Watts CFG0010/105W CPUs, 16 DIMMs) - 340 Watts CFG0011/105W CPUs, 8 DIMMs) - 320Watts	Complete steady power consumption including IPMC
Transition from early to steady levels, sec	0s	-

9.10 BIOS Boot Configuration Parameters

The IPMC allows storing BIOS setup variables in the NVRAM area of the BIOS flash. When BIOS starts, it first copies its own set of NVRAM parameters into memory. Then it reads parameters from the IPMC, adding new parameters to the parameter set in memory, and deleting or modifying existing ones. During runtime, only the memory copy of the parameter set is used.

The parameters changed and stored in the BIOS setup menu are automatically saved back into the non-volatile memory of the IPMC. The IPMI command being used to manage the boot configuration variables is called Set/Get System Boot Options together with parameter #100. For details, see *System Boot Options Commands on page 235*.

Storing BIOS Boot environment variables in IPMC non-volatile memory has the advantage, which can be set by the ShMM or across HPI applications as well. The system manager may decide from which boot device the blade should boot from.

The boot configuration parameters are stored as sets of <parameter name> and <value> pairs. They can be easily enhanced and there are no dependencies between different versions of IPMC firmware and payload firmware. The IPMC provides a set of boot configuration parameters and the payload firmware just initializes those he knows about.

The boot options need to be stored as a sequence of zero terminated strings. The following table describes in detail about format of the boot options to be used when setting or reading the System Boot Options parameter #100.

Table 9-11 IPMC Boot Parameter Storage Format

Byte	Description
0-1	Number of bytes used for boot parameters (LSB first) The number of bytes must be calculated and written into these two bytes by the software, which writes into the storage area. The values `0x0000` and `0xFFFF` indicate that no data has been written to the storage area. If you are reading from the storage area and you find any of these two values, your software should assume that no boot firmware options have previously been written to the storage area.
2-n	Boot Parameters data The boot parameters are stored as ASCII text with the following general format: `<name>=<value>`, where all name/value pairs are separated by a zero byte. The end of the boot parameter data is indicated by two zero bytes. Allowed and supported name/value pairs are blade specific.
N+1 - n+2	16 bit checksum over the boot parameters data section (LSB first).

When writing or reading from the storage area, you can only read or write chunks of 16 bytes at a time. For this reason, the IPMC memory is divided into numbered blocks of 16 bytes which need to be addressed individually. For this purpose the "block selector" field in the request data field is used.

9.11 Asynchronous Event Notification

To make payload applications to be informed about graceful shutdown/reboot requests, the "FRU Activate (Deactivate)" and "FRU Control (Graceful Reboot)" commands messages are routed as a LUN2 message to payload interface.

The provided payload application has registered to these commands via OpenIPMI library, which gets informed and can take all necessary actions before the payload is gracefully rebooted/shut-down.

Graceful Reboot and Graceful Shutdown is also communicated to the Intel CPU via internal communication channel.

9.12 Serial Line Selection

The ATCA-7480 provides two serial interfaces from payload. By default, the first is routed to the front connector and the second to the RTM. In addition, there is an IPMC debug interface, which can be routed either to the front or to the RTM (this function is just available if the RTM provides a serial connector at the front).

The IPMC provides an OEM command called `Set/Get Serial Output` to be used to influence this serial interface routing default. The serial line selection is implemented non-persistently to ensure that the serial interfaces always can be accessed easily after power-up.

9.13 BIOS Boot Bank Selection

The ATCA-7480 provides redundant payload boot flashes for manual and automatic crisis recovery.

The general concept is that there is always an active and a standby SPI flash device. The role of the two devices can be reversed by the FPGA; for this to work, the FPGA has to drive the chip select signals to the SPI flashes. The final decision on which of the two devices is active and standby is done by the IPMC.

The BIOS Boot Bank Selection is implemented such that swapping the SPI flashes is not in effect immediately. To ensure that the active BIOS bank cannot be overwritten at all (BIOS upgrades always can just access the backup boot bank), the boot bank selection is masked with a payload reset. Therefore, swapping the boot bank is possible with the following steps only:

- Swap the BIOS boot banks
- Reset the payload

NOTICE
Be aware that swapping the BIOS boot bank is active only after payload reset.

The IPMI command, `Set/Get System Boot Options` together with the parameter #96 can be used to specify the BIOS boot bank from which the payload shall boot from persistently. For details, see *System Boot Options Commands on page 235*.

9.13.1 Boot Bank Sensor

The ATCA-7480 provides a Boot Bank Sensor, illustrating from which BIOS Boot Bank the boot firmware has last booted. For details, see *Boot Bank Supervision Sensor on page 306*.

9.13.2 Fail Safe Logic

Fail Safe is a mechanism, implementing automatic BIOS boot bank crisis recovery. It observes the BIOS boot phase to swap the BIOS boot banks and to reset the processor in case the boot firmware hangs accidentally.

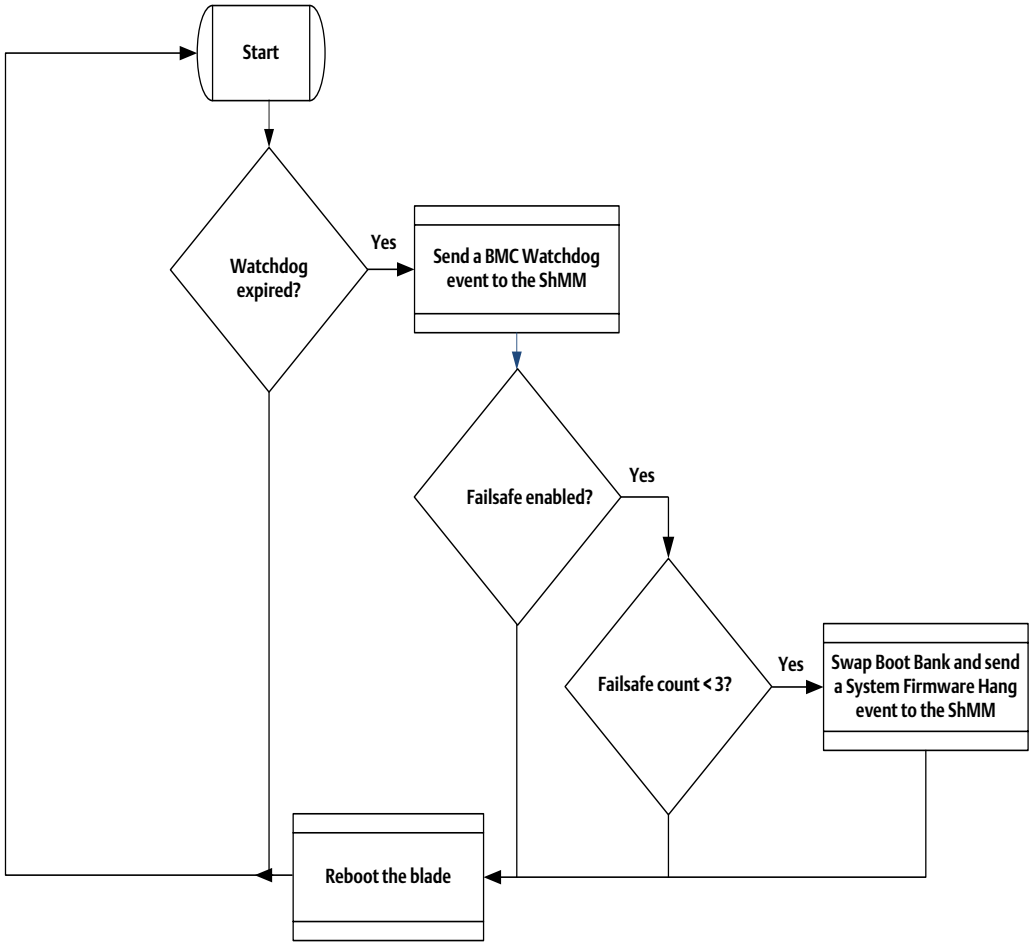
Fail Safe can be enabled or disabled at any time with:

- IPMI OEM command called `Set/Get Feature Configuration` and parameter #224. For details, see *Set Feature Configuration on page 259*.
- BIOS setup menu

Typically, Fail Safe is used to protect a BIOS firmware upgrade to recover, even when the boot image programmed does not work, is damaged, or has an unpredictable error.

Fail Safe is implemented within the IPMI management controller. In case the firmware does not boot and the BMC watchdog expires, the IPMI management controller will swap the boot banks before resetting the CPU. Thus the blade can recover by booting from its redundant boot flash, which contains the old active firmware image, which did work before firmware upgrade.

Figure 9-4 Fail Safe Logic Diagram



Fail Safe in general can recover from scenarios:

- Missing or defect boot block
- Firmware image has a bad checksum

When the Fail Safe logic is triggered as a result of the BMC Watchdog timeout, a System Firmware Progress event is logged as follows:

```
Sensor Type: 0x0F (System Firmware Progress)
Event Reading Type Code: 0x6F (Sensor Specific)
Event Data Byte 1: 0xA1 (System Firmware Hang)
Event Data Byte 2: 0x00 (CPU instance)
Event Data Byte 3: 0xXX (Failed Boot Bank ID: 0=Bank A; 1=Bank B)
```

The Fail Safe logic makes three attempts to boot the payload successfully. After three attempts, the Fail Safe logic is automatically disabled and the boot bank is left in the original state (before the payload was booted).

Payload software is able to detect when failsafe was activated during last boot. For details, see *Table 8-26*.

By default, Fail Safe is disabled.

9.14 Glue Logic FPGA Flash Selection

The ATCA-7480 provides redundant FPGA flashes for both manual and automatic crisis recoveries.

The general concept is that there is always an active and a standby SPI flash device. The role of these two devices can be reversed by the IPMC; for this to work, the IPMC has to drive the chip select signals to the SPI flashes. The final decision about which of the two devices is active and standby is made by the IPMC.

Due to the fact that the Glue Logic FPGA is powered by management power, the IPMC needs to control the Glue Logic FPGA during power-up.

The FPGA Bank selection is implemented such that swapping the SPI flashes is in effect immediately. Nevertheless due to the FPGA is already loaded during power-up, the SPI flash selection does not enforce the FPGA to reload. Furthermore, in case of the payload, powered (M4) FPGA cannot be loaded neither.

Therefore, swapping FPGA bank is possible only with the following steps:

1. Swap the FPGA banks
2. Power-cycle the payload

The IPMI command `Set/Get System Boot Options` together with the parameter #96 can be used to specify the FPGA boot bank from which the payload shall boot persistently. For details, see *System Boot Options Commands on page 235*.

9.14.1 Boot Bank Sensor

The ATCA-7480 provides a Boot Bank Sensor, illustrating from which FPGA Bank the FPGA has booted last. For details, see *Boot Bank Supervision Sensor on page 306*.

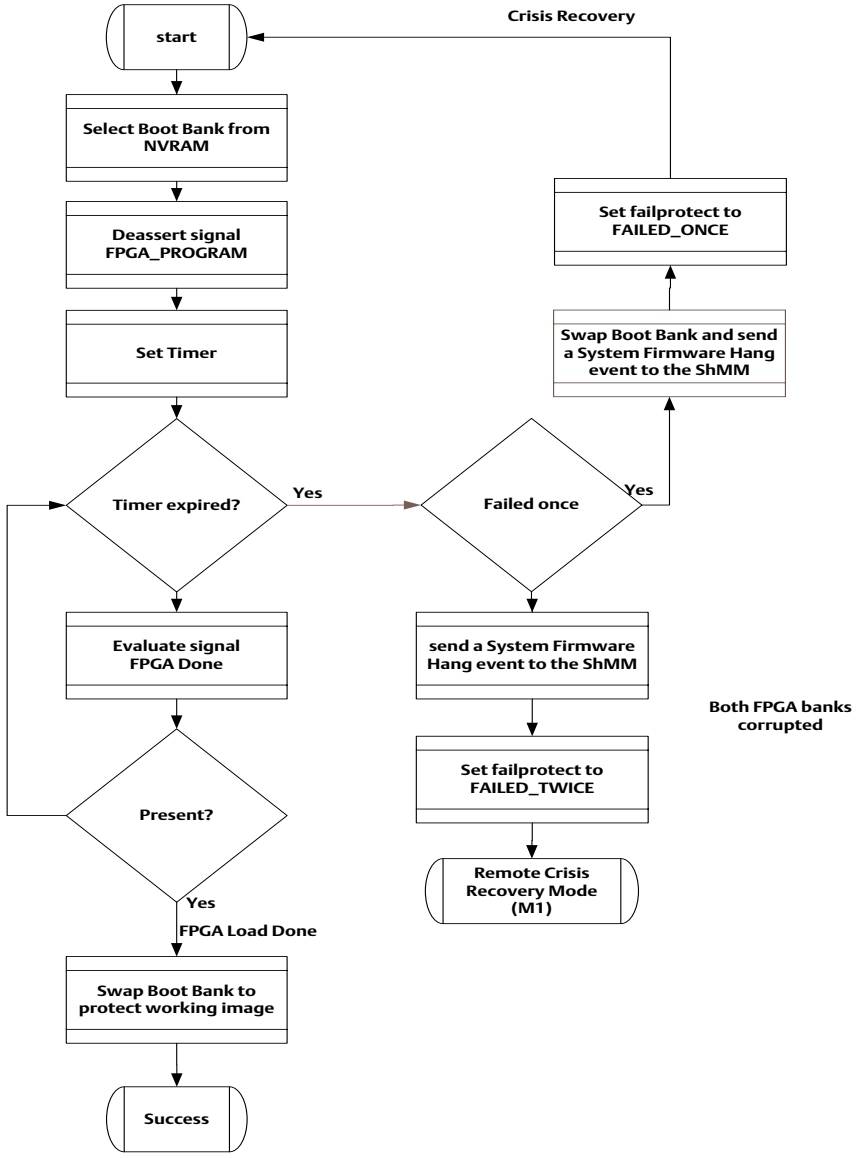
9.14.2 Fail Protect Logic

Fail Protect is a mechanism, implementing automatic FPGA bank crisis recovery. It observes the FPGA boot phase, to swap the FPGA banks and to reload the FPGA, in case of the FPGA firmware hangs accidentally.

Fail Protect can be enabled or disabled at any time using an IPMI OEM command called `Set/Get Feature Configuration` and parameter #224. For details, see *Set Feature Configuration on page 259* or BIOS setup menu.

During initial power-on, the IPMC selects the FPGA bank stored in NVRAM and evaluates the `FPGA DONE` signal. If the provided signal is not asserted, the IPMC selects the FPGA backup bank and tries to load the FPGA again.

Figure 9-5 Fail Protect Logic Diagram



In case both SPI flashes are corrupted, the IPMC enters remote crisis recovery mode and moves to hot-swap state M1, waiting for a FPGA firmware upgrade initiated from the ShMM.

To ensure that there is no possibility to accidentally overwrite both FPGA flashes with wrong images not working, FPGA Fail Protect is implemented such that the active FPGA bank is protected always by de-selecting it (only the backup firmware bank can be upgraded).

When the Fail Protect logic is triggered as a result of the timer expiry, a System Firmware Progress event is logged as follows:

```
Sensor Type: 0x0F (System Firmware Progress)
Event Reading Type Code: 0x6F (Sensor Specific)
Event Data Byte 1: 0xA1 (System Firmware Hang)
Event Data Byte 2: 0x00 (CPU instance)
Event Data Byte 3: 0xXX (Failed Boot Bank ID: 0=Bank A; 1=Bank B)
```

Payload software is able to detect when Fail Protect was activated during last boot. For details, see *Table 8-26*.

By default, Fail Protect is activated.

9.14.3 Remote Crisis Recover Mode

This mode is entered when both FPGA flashes are corrupted and the FPGA cannot be loaded. The IPMC moves into hot-swap state M1 and waits for subsequent firmware upgrades initiated from ShMM.

9.15 Settable Graceful Shutdown Timeout

The IPMI command, `Set/Get System Boot Options` together with the OEM parameter #98 can be used to specify the timeout for Graceful Shutdown persistently. For details, see *System Boot Options Commands on page 235*.

By default, Graceful Shutdown persistently value is set to 10 seconds.

9.16 Local System Event Log (SEL)

The Penguin Edge IPMC supports a local SEL. The local SEL size is configured to hold 1K entries in a circular FIFO buffer. Once the circular buffer is full, the next SEL entry will overwrite the oldest SEL entry in the buffer. All events are automatically logged locally to the local SEL before being passed to the Shelf's SEL, which includes all events that occur from the local MMC.

To support the local SEL, a software emulated RTC (Real Time Clock) is enabled which upon startup requests the local time from the shelf manager by sending an IPMI standard command, `Get SEL Time`. Once the initial time is received, the IPMC maintains the time locally and no further synchronization is performed with the shelf manager.

Ruggedized ATCA-7480 Information

A.1 Ruggedized ATCA-7480 Overview

The ruggedized configuration of the Penguin Edge™ ATCA-7480 is a COTS dual-processor server blade with a specially designed alignment block that enables the blade to be secured in a shelf, like the ruggedized configuration of the AXP1440, with captive screws for rugged environments. Careful component choices have been made for an extended product life cycle.

The ruggedized ATCA-7480 is electrically identical to the ATCA-7480 blade. References to the ATCA-7480 in this manual also apply to the ruggedized configuration.

A.2 Mechanical

The following figures show the location of the specially designed Zone 2 alignment block, alignment block drawing, captive screws in the shelf, and alignment block/captive screw relationship.

Figure A-1 Location of the Alignment Block on the Ruggedized ATCA-7480 Blade

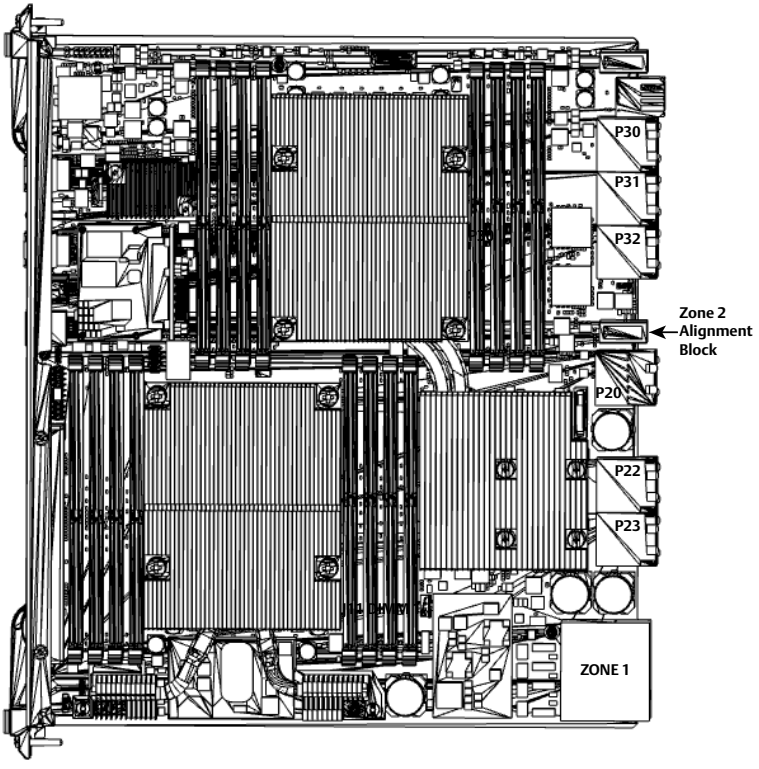


Figure A-2 ATCA Blade Alignment Block

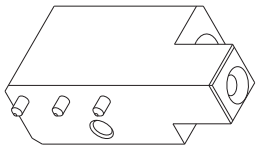


Figure A-3 Captive Screws in the AXP1440-D Shelf

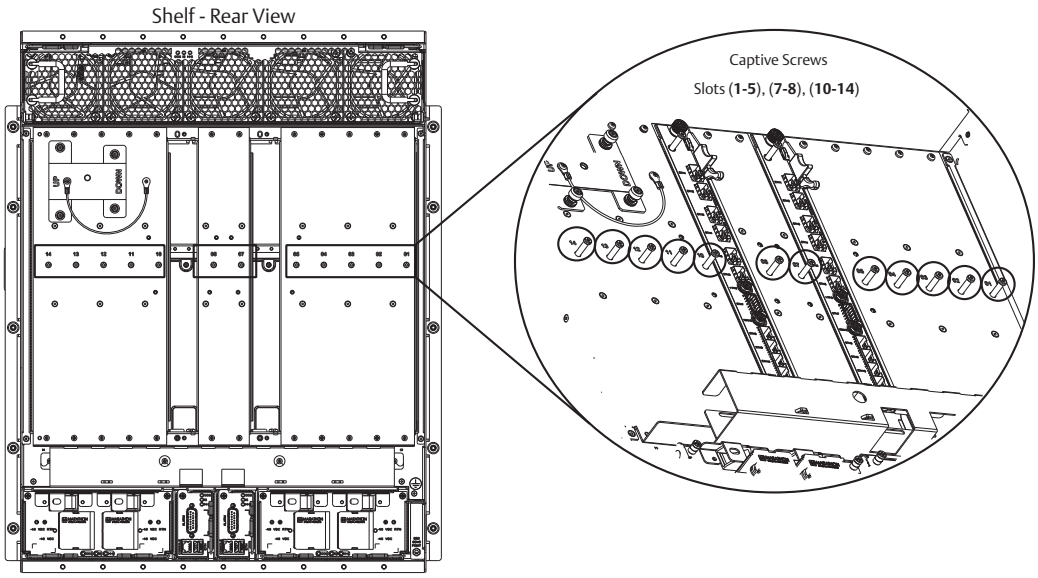
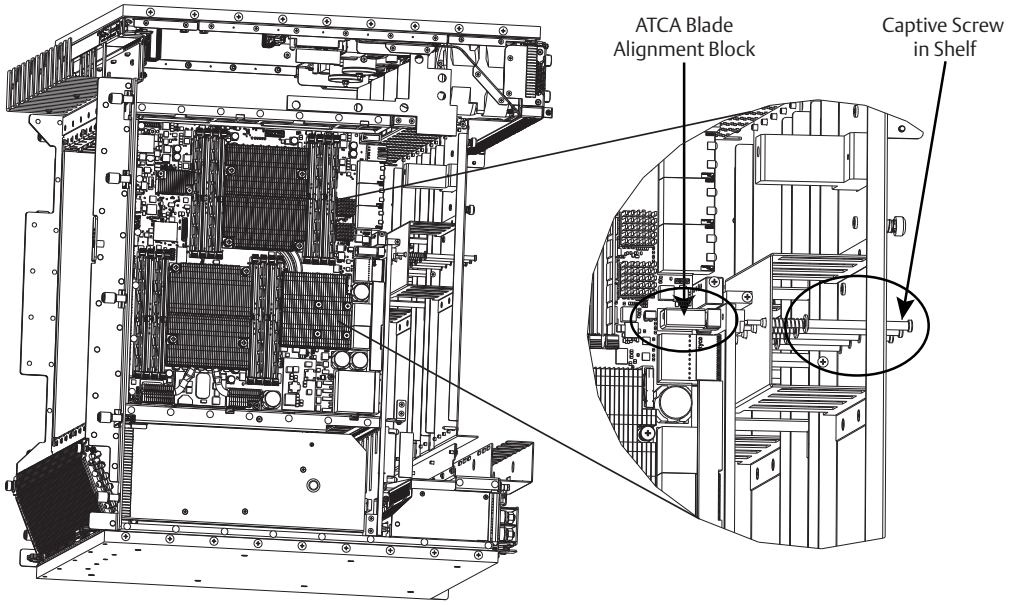


Figure A-4 ATCA Blade Alignment Block and Captive Screw in the AXP1440-D Shelf



A.3 Ordering Information

Please reference the data sheet for ATCA-7480 blade variants and blade accessories available. Refer to the *Appendix B, Related Documentation on page 327* or consult your local Penguin Solutions sales representative for the availability of other variants.

For technical assistance, documentation, or to report product damage or shortages, contact your local Penguin Solutions sales representative or visit *https://www.penguinsolutions.com/edge/support/.*

Related Documentation

B.1 Penguin Solutions Documentation

The documentation listed is referenced in this manual. Technical documentation can be found by using the Documentation Search on our Support web page at *https://www.penguinsolutions.com/edge/support/* or you can obtain electronic copies of Penguin Solutions documentation by contacting your local sales representative.

Table B-1 Penguin Solutions Documentation

Document Title	Document Number
ATCA-7480 Data Sheet	ATCA-7480-DS
ATCA-7480 Quick Start Guide	6806800T34
ATCA-7480 Safety Notes Summary	6806800T27
Basic Blade Services Software on ATCA-7480 Programmer's Reference	6806800T30
ATCA-748X MMOD-SSDKIT Quick Start Guide	6806800T15

B.2 Manufacturers' Documents

For additional information, refer to the following table for manufacturers' data sheets or user's manuals. As an additional help, a source for the listed document is provided. Please note that, while these sources have been verified, the information is subject to change without notice.

Table B-2 Manufacturer's Documents

Company	Document Title
Intel	6300ESB I/O Controller Data sheet 82546EB/GB Gigabit Ethernet Controller Documentation 6700PXH 64-bit PCI-to-PCI bridge Data sheet E7520 Memory Controller Data sheet IPMI V1.5 Specifications Intel® Xeon™ Processor Technical Documents
LSI Logic	LSIFC929XL Dual-Channel PCI-X to Fibre Channel Controller Technical Documents
SMSC	LPC47S422 Enhanced Super I/O Controller Data sheets and Application Notes

B.3 Related Specifications

For additional information, refer to the following table for related specifications. As an additional help, a source for the listed document is provided. Please note that, while these sources have been verified, the information is subject to change without notice.

Table B-3 Related Specifications

Organization	Document Title
PCI-SIG	PCI Local Bus Specification Revision 2.2 PCI-X Addendum to the PCI Local Bus Specification 1.0
PICMG	PICMG 3.0 Revision 2.0 Advanced TCA Base Specification PICMG 3.1 Revision 1.0 Specification Ethernet/Fiber Channel for AdvancedTCA Systems

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